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July 8, 2011

Soitec report

1.0 Safe harbor notice

The process flows utilized in this report were developed in concert with industry experts and are believed to be reasonable projections of industry practices for 22nm System On a Chip (SOC) production. The process flows were entered into the commercially available IC Knowledge - Strategic Cost Model for all cost projections. The Strategic Cost Model uses a set of algorithms and industry data complied from a variety of primary and secondary sources. The model results are believed to be reasonable estimates of industry costs. Changes in technology, markets conditions, equipment or matreial costs, practices from company to company or other factors could cause results to differ from the results projected here. These projected results are forward looking statements subject to significant risks and uncertainties and actual results may differ materially from the forward looking statements.

2.0 Background

Soitec is a world leader in the manufacture of Silicon On Insulator (SOI) wafers. Soitec engaged IC Knowledge to evaluate the cost of Fully Depleted SOI (FDSOI) versus bulk CMOS process flows at 22nm.

Soitec provided IC Knowledge with some basic parameters for the comparison. The 22nm bulk process was to be assumed to have three threshold voltages, dual gate oxides, a full complement of mobility enhancing stressors and be suitable for SOC applications.

The FDSOI processes to be evaluated are to include three threshold voltages, high-k metal gates with two work functions. Further inputs included n+ and p+ back gate implants into the n-well and p-well implants under the buried oxide, access to the n-well and p-well, two shallow trench isolation depths, ESD devices in a bulk area, implanted or in-situ doping and a $500 cost for the SOI substrate.

All processes assume gate-last high-k metal gate (HKMG) and 8 metal layers.

3.0 Methodology

Working with a process consultant and Soitec - IC knowledge developed 22nm bulk CMOS, FDSOI with implant doping, and FDSOI with in-situ doping process flows. The flows were initially developed by IC Knowledge in consultation with our process consultant and then submitted to Soitec for review and comment. The flows were modified as required until three consensus process flows were developed. The three process flows are believed to be representative of state-of-the-art industry practices.

A comparison of the complexity of the three process flows is illustrated in table 1.

Table 1. Process complexity comparison.

Process factor	Bulk	FDSOI - implant	FDSOI - in-situ
Photo masks	47	34	32
Implants	63	17	15
Steps	328	250	241

As can be seen from table 1 FDSOI offers the potential for significant reduction in process complexity. It should be noted here that the masks for implants are non-critical masks and therefore relatively inexpensive. The reduction in a number of relatively inexpensive implant masks and implants has to be contrasted against the cost of the SOI starting wafer.

The resulting process flows were entered into the commercially available IC Knowledge - Strategic Cost Model revision 1106. A 30,000 wafer per month wafer fab operating in Taiwan was simulated for the 2012 time frame. Please note that a "22nm" process for ASICs is assumed to be a 38nm metal-one half-pitch process as defined by the International Technology Roadmap for Semiconductors (ITRS) for the purposes of modeling.

At a high level the fabrication costs for a wafer may be broken down into three main categories, material, labor and overhead costs. The next three sections discuss these costs in more detail.

3.1. Material costs

Material cost is the cost of the starting substrate. There is a table in the model that lists for each process; the starting substrate type - raw, epitaxial or SOI, there is also cost data for each of these substrate types by type, wafer size and year. Based on the process selection and year the appropriate substrate cost is determined. Since virtually all semiconductor companies purchase starting substrates, substrate costs are based on open market wafer pricing obtained by IC Knowledge from sources in the commercial wafer supply business.

For 2012 the pricing for epitaxial wafers and SOI wafers are $130, and $500 respectively.

3.2. Labor costs

Labor costs refers to the direct labor (people who actually process the wafers). For the three flows of interest the number of mask layers has been determined. Based on labor hours per mask productivity data from studies done at Berkeley and IC Knowledge data the labor hours required to make a wafer can be calculated. A table in the model contains labor rates by country and by year for the semiconductor industry. Sources for this data include the bureau of labor statistics, IC Knowledge and SEMATECH. The combination of labor rate (which depends on the country selected) and labor hours allows the labor cost per wafer to be determined.

3.3. Overhead

Overhead - overhead is the most complex cost category and encompasses all of the other costs.

- Depreciation - the largest single cost for advanced fabs is typically depreciation. To calculate depreciation costs, hidden tables in the model are utilized. For each process of interest the developed process flows are used to determine how many times each process requires each of 64 different equipment operations. The hidden tables include the cost for each of the 64 differ-

ent types of equipment (this data is process generation specific), what the equipment throughput is for each piece of equipment (this data is process generation specific), and finally the footprint of each piece of equipment (this data is wafer size specific). In the background of the model the process selection and the fab capacity (in this case 30,000 wafers per month) are used to determine the equipment set required, the equipment set cost and the fab size needed to house the equipment. Cost per square foot numbers (wafer size specific) are then used to calculate the fab and building costs. The total capital investment, the year the fab was built (assumed to be a new fab) and the depreciation rules (five year straight line) are then used to calculate the depreciation costs for the total wafer fab.

- Indirect Labor - indirect labor includes supervisors, engineer and technicians. Berkeley survey data as well as IC Knowledge data on indirect labor productivity and profiles is used to calculate the required indirect labor by category. Indirect labor salary data from salary surveys along with the country selected are then used to calculate indirect labor costs.
- Maintenance - IC Knowledge data on maintenance costs by equipment generation and equipment set are used to calculate equipment maintenance costs.
- Monitor wafers - data on monitor wafer usage combined with data from wafer suppliers on monitor wafer costs is used to calculate monitor wafer costs.
- Facility Costs - based on the calculated size of the cleanroom and the facility as well as calculations of the electricity required based on wafer size and volume and water use based on the wafer volume and process flow, IC Knowledge uses proprietary data to calculate facility costs.
- Consumable costs - the single largest consumable cost for advanced designs is the reticle set cost. Based on the number of mask layers for each process, data from the industry and SEMATECH and other industry sources on cost per reticle versus linewidth and SEMATECH and customer data on the number of exposures per reticle that are typically performed for logic, DRAM and ASIC processes, the reticle cost per wafer is calculated. Similar calculations are performed for gases, cleaning chemical, photochemicals, CMP and other consumable items. In this specific case where foundry fabrication is assumed mask amortization is not included in the wafer cost because foundry process mask reticle sets are typically pre-paid.

The resulting unyielded wafer cost is then divided by the wafer yield calculated based on the number of mask layers and Berkeley and IC Knowledge data on yield per mask layer.

The calculated wafer costs have been validated against, IC Knowledge and customer wafer cost data collected from fabs throughout the industry.

4.0 Calculated costs

The resulting costs from the Strategic Cost Model analysis are presented in table 2:

These costs are believed to be representative of a new, well run, 30,000 wafers per month foundry fab located in Taiwan.

Table 2. Fabricated wafer cost

Cost factor	Bulk	FDSOI - implant	FDSOI - in-situ
Depreciation	$1,857.71	$1,666.09	$1,623.03
Equipment maintenance	$443.12	$395.10	$384.48
Direct labor	$34.79	$25.17	$23.69
Indirect labor	$67.91	$49.13	$46.33
Facilities	$199.32	$163.97	$157.90
Material	$130.00	$500.00	$500.00
Consumables	$227.58	$213.39	$209.81
Monitor wafers	$17.83	$20.79	$20.48
Total unyielded wafer cost	$2,978.3	$3,033.60	$2,965.70
Wafer yield	97.70%	98.30%	98.40%
Yielded wafer cost	$3,049.10	$3,085.70	$3,013.60

5.0 Discussion

To-date SOI usage in the industry has been for partially depleted SOI processes where the cost of the SOI substrate and relatively similar process requirements to bulk incur a significant cost penalty for SOI adoption. The potential performance advantage of SOI has not been sufficient to offset the cost disadvantage and SOI has only been able to achieve relatively modest market penetration. FDSOI offers the potential for significant process simplification making FDSOI cost competitive while simultaneously offering performance improvements.

As previously noted the cost of implant masks and implants is relatively low. The FDSOI flows both dramatically decrease the number of masks and implants required as well as total steps. The cost of the steps that are eliminated then has to be compared to the cost adder for the FDSOI substrate. The results in table 2 show that the cost savings from process simplification are sufficient to bring a FDSOI flow to approximate cost parity versus a bulk flow.

There are two areas this analysis does not consider:

The first is that FDSOI offers potential performance improvements in leakage and speed versus a bulk process particularly at advanced process nodes. The analysis in the this report is strictly a cost based analysis. The potential exists to achieve a small cost saving and improved performance by moving to FDSOI at 22nm.

The second area is that this report does not compare FDSOI to bulk multi-gate transistor processes. Intel has recently announced that they are moving to a bulk multi-gate process at 22nm. Multi-gate processes also offer the potential for process simplification and improved performance without the expense of the FDSOI starting wafer and in our opinion represent the more likely competitor to FDSOI at advanced process nodes.

6.0 Conclusion

Adoption of SOI has historically been slowed by the high cost of the SOI substrate and resulting increased cost per fabricated wafer. FDSOI (as opposed to partially depleted SOI used to-date) offers the potential for significant process complexity reduction. As has been shown in this analysis FDSOI offers approximate cost parity at 22nm. Although not examined here FDSOI will

likely offer a significant performance advantage at 22nm over bulk as well, making FDSOI an attractive alternative for advanced process nodes.