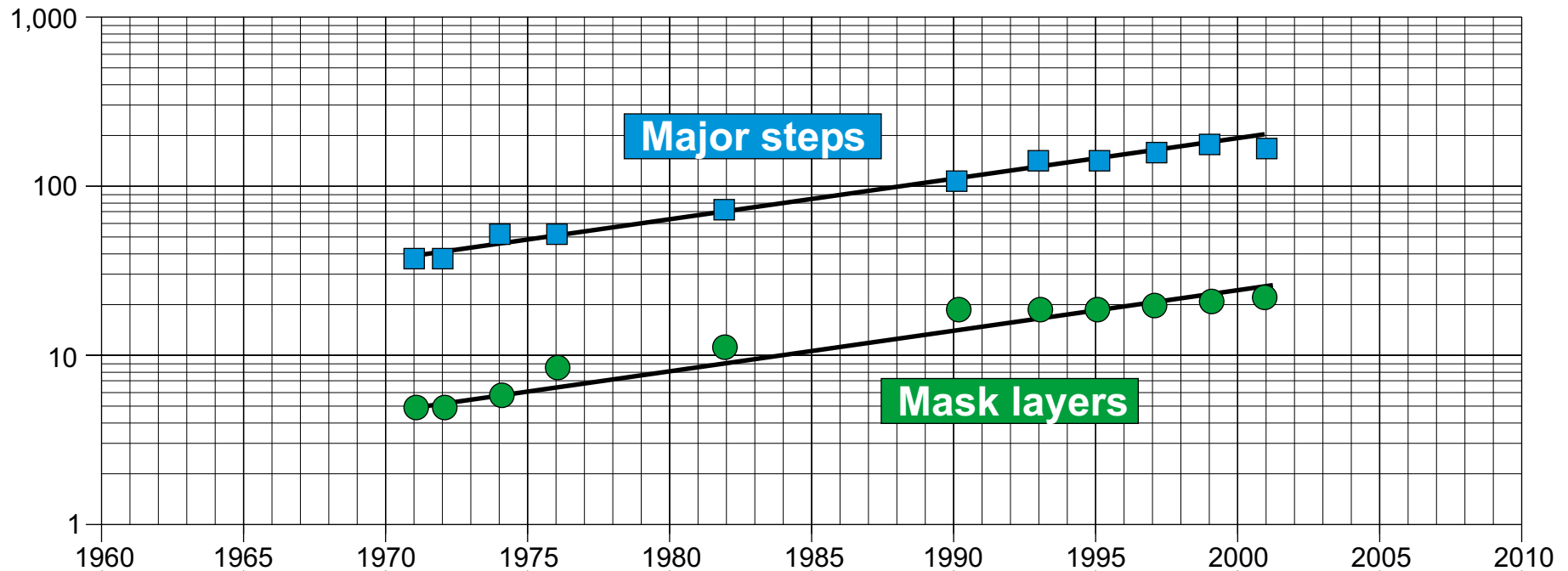


MOS Logic Process Trends



Process type	PMOS	NMOS		CMOS																						
Substrate	Raw			Epi			SOI																			
Linewidth (μm)	8		6		3		1.5		0.8		0.5		0.35		0.25		0.18		0.13		0.09		0.065		0.045	
Wells	None			1-diffused			2-diffused		2-retrograde																	
Isolation	Etched oxide			LOCOS			STI																			
Gate oxide	SiO ₂										SiO _x N _y		HfO ₂ /ZrO ₂													
Gate	Al			Poly-Si																						
Etch	Gate	Wet			Dry																					
	Contact	Wet			Dry																					
	Metal	Wet			Dry			Damascene																		
Contact metal	None			TiSi ₂		CoSi ₂		NiSi																		
Barrier metal/Plug	None										TiN/W															
Interconnect metal	Al			AlCu		AlCuSi		AlCu		Cu																
Interconnect layers	1			2		3		4		5		6		6		7		8		9						
Inter-level dielectric	None			SiO ₂			k<2.7		k<2.4																	
Planarization	None			Spin-On/Etch-Back		CMP																				