Current Technical Trends: Dual Damascene & Low-k Dielectrics

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Introduction

As CMOS transistor scaling proceeds into the deep sub-micron regime, the number of transistors on high performance, high density ICs is in the tens of millions, in accordance with the historical trend of Moore's Law. The signal integration of this many active elements has necessitated that such ICs feature as many as eight layers of high density metal interconnect. The electrical resistance and parasitic capacitance associated with these metal interconnections has become a major factor that limits the circuit speed of such high performance ICs. It is also the fundamental motivating factor causing the semiconductor industry to move away from Aluminum interconnect metal with Silicon Dioxide dielectric between the metal lines, to Copper metal and low-k dielectric materials. Copper reduces the resistance of the metal interconnect lines (and increases their reliability), while low-k dielectrics reduce the parasitic capacitance between the metal lines. These new materials are employed in a fabrication process called "Dual Damascene" which is used to create the multi-level, high density metal interconnections needed for advanced, high performance ICs. The initial transition to Dual Damascene employed Copper metal with traditional Silicon Dioxide dielectric. More recently, the trend has moved toward the replacement of Silicon Dioxide dielectric with new low-k dielectric materials.

The transition to porous low-k dielectrics, combined with copper metallization, poses a significant integration problem for the Dual Damascene process. Although either the trench or the via can be etched first in Dual Damascene, most semiconductor manufacturers have chosen to adopted the via-first approach. However, this methodology, and other aspects of the Dual Damascene process, particularly barrier materials, may be forced to undergo revision as the unique and frequently fragile properties of low-k dielectrics are taken into consideration.

In order to appreciate the details of this integration challenge, it is useful to review the processing options available for the formation of Dual Damascene structures.

Because Copper does not form a volatile by-product, it is very difficult to etch, and therefore Copper metallization schemes cannot be realized using the traditional subtractive etching approach used to form Aluminum metal lines. The Dual Damascene technique overcomes this problem by etching a columnar hole, followed by a trench etch into the inter-layer dielectric (ILD), and then filling both structures with Copper which is subsequently polished back (using Chemical Mechanical Polishing (CMP)) to the surface of the ILD. The result is a vertical Copper via connection and an inlaid copper metal line.

A key issue here is which of the two etches in the Dual Damascene process (the via etch or the trench etch) should be performed first, as well as the selection of an appropriate barrier material.

The Trench-First Approach

In this methodology, the wafers are coated with photoresist, lithographically patterned, and an anisotropic dry etch cuts through the surface hard mask (typically plasma Silicon Nitride), and down through the low-k dielectric, stopping on the embedded etch stop layer (also typically Silicon Nitride). The photoresist is then stripped, leaving behind a trench in the ILD.

The surface hard mask on top of the ILD is required to protect the ILD from the photoresist stripping process. This is because the low-k materials that form the ILD are susceptible to the same chemistries that strip photoresist. In addition, the surface hard mask acts as a CMP stop during subsequent copper polishing [1].

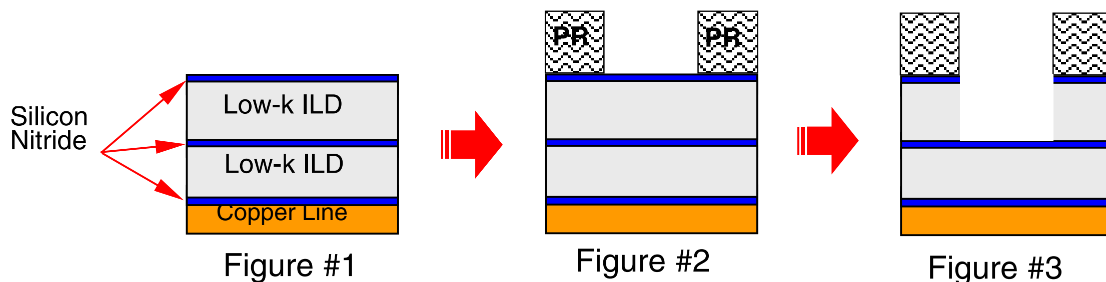

Figure #1 Figure #2 Figure #3

Next, photoresist is again applied to the wafers and lithographically patterned. The via etch then cuts through the embedded etch stop layer and down through the ILD, to the final Silicon Nitride barrier located at the bottom of the via. The bottom barrier is then opened with a special etch and the photoresist is stripped.

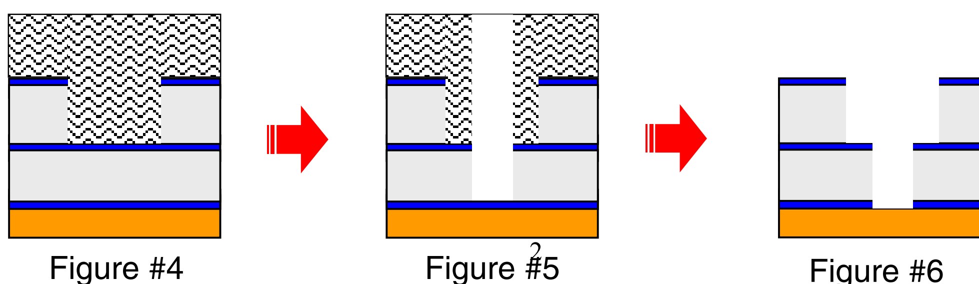

Figure #4 Figure #5 Figure #6

Next, a thin Tantalum barrier is deposited which lines the Dual Damascene structure and acts as a barrier to prevent the Copper (deposited in the next operation) from diffusing into the ILD.

A Copper seed layer is next deposited using PVD and the bulk Copper is deposited via electroplating. The Copper is then polished back using CMP to the surface of the trenches, a thin Silicon Nitride barrier is deposited on top of it, and the Dual Damascene structure is completed.

The major drawback of the trench-first approach is that after the trench has been etched, the photoresist that is applied for the via step will completely fill these trenches (refer to figure # 4). Thus, the photoresist can be said to have "pooled" in the trenches, creating local regions of extra thick resist right in the areas where the vias are to be patterned. Forming the very fine via structures in such thick resist is extremely difficult, and the processing margin for via formation becomes untenable at very small geometries. As a result, the trench-first approach to Dual Damascene formation was largely abandoned at the 0.25µm technology node.

The Via-First Approach

In this methodology the wafers are first coated with photoresist and then lithographically patterned. Next, an anisotropic etch cuts through the surface hard mask and etches down through the ILD and the embedded etch stop, and stops on the bottom Silicon Nitride barrier. It is important that the via etch does not break through this bottom layer, because if it does, the via etch will sputter the Copper located beneath the barrier up into the unprotected via hole. The Copper will then quickly diffuse into the ILD, leading to device failure.

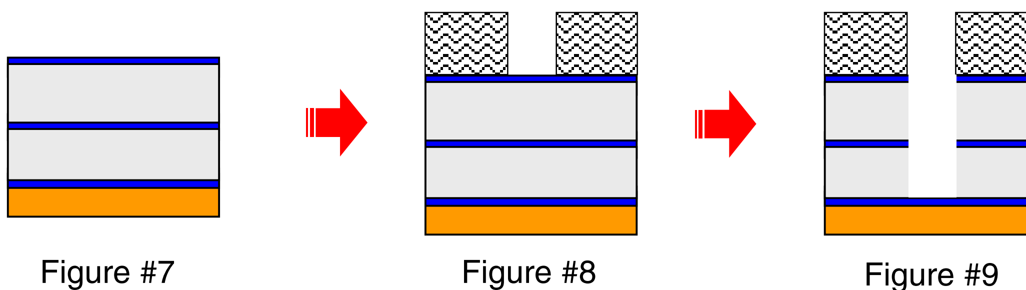

Figure #7 Figure #8 Figure #9

Next, the via photoresist layer is stripped, and the trench photoresist is applied and lithographically patterned. Some of the photoresist will remain in the bottom

of the via (refer to figure # 10), and prevent the lower portion via from being over-etched during the trench etch process.

An anisotropic etch then cuts through the surface hard mask and down through the ILD, stopping at the embedded hard mask. This etch forms the trench. The photoresist is then stripped and the Silicon Nitride barrier at the bottom of the via is opened with a very soft, low-energy etch that will not cause the underlying Copper to sputter into the via.

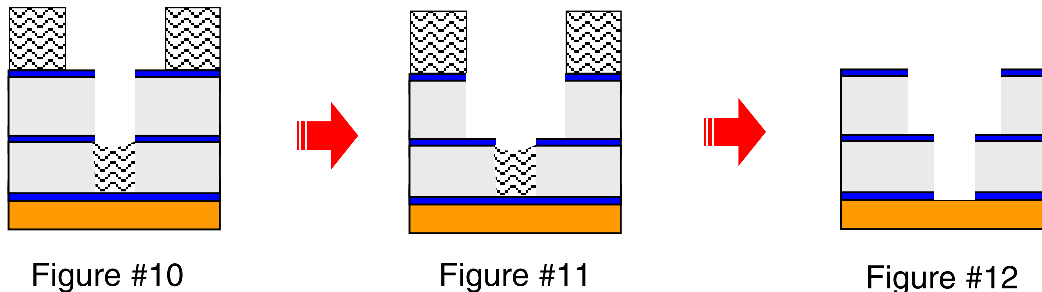

Figure #10 Figure #11 Figure #12

Finally, the Tantalum, Copper seed and bulk Copper are deposited and planarized using CMP, as previously described in the trench-first approach.

The via-first approach has been widely adopted for small geometry devices because it avoids the photoresist pooling effect that occurs when the trenches are formed before the vias. The only pooling of photoresist that occurs happens at the bottom of the already formed via, and this has the beneficial effect of shielding the lower via from the trench etch [2].

Integration Challenges

Although the via-first approach has been very successful for Dual Damascene implementation in Silicon Dioxide, Fluorinated Silicate Glass (FSG), and some early versions of low-k materials, it faces a severe challenge when used with ultra low-k materials. This is due to the fact that in the via-first approach, residual photoresist remains behind in the bottom of the via during the trench etch, as previously mentioned. However, due to the highly porous nature of ultra low-k dielectrics, this residual photoresist may be absorbed by the ILD, contaminating it, and altering its k value.

This may necessitate the return to a modified trench-first approach to Dual Damascene fabrication. However, even this approach is not without risk, because in the trench-first approach photoresist also pools in the open trench structure prior to via patterning (refer to figure #5). In addition, the use of a trench-first

methodology at device nodes below 0.25µm would require the development of a thin resist imaging process in order to accommodate the patterning of fine via structures through the pooled resist in the trenches.

Further problems concerning ultra low-k dielectrics arise in regard to Chemical Mechanical Polishing. Most low-k films are hydrophilic in character, and it is critical that the surface hard mask, located on the top of the ILD stack, shield the ILD from moisture during the Copper CMP process, as well as protect the ILD from aggressive cleans. It must also block Copper diffusion, and act as a CMP stop.

Furthermore, when the barrier material is used in the middle of the ILD stack, it must behave as an embedded etch stop. This requirement means that the barrier etch rate must be significantly slower than that of the ILD in order to ensure adequate etch selectivity.

Currently the Silicon Nitride is the material employed to perform these multiple roles. However, as the industry drives toward lower and lower ILD k values, the permittivity of Silicon Nitride ($6<k<8$) becomes unacceptable. Its relatively high permittivity undesirably raises to the overall permittivity of the ILD stack, compromising the stack's ability to mitigate electrical delay. Other materials that have lower k values, such as amorphous SiC:H, have been investigated and show considerable promise as substitutes for Silicon Nitride. SiC:H has good adhesion characteristics, is chemically inert, and therefore makes an excellent CMP stop [3]. It also forms a good etch stop layer due to its slow etch rate relative to low-k materials, and is a good barrier to moisture and Copper diffusion.

However, the barrier material is a central component of the low-k/Dual Damascene structure, and changing something so fundamental cannot be done without exhaustive study, and will probably only occur if it becomes absolutely necessary. This issue is further clouded by the reality that the precise character of the ILD material that will be used for future devices is far from being decided. There are many competing and very different candidates for the role of low-k dielectric ILD (spin-on versus CVD; fluorinated versus non-fluorinated organic polymers, etc.), and this issue will need to be settled before an entirely new barrier material can implemented. Indeed, the proliferation of low-k materials is a chief obstacle to the resolution of the Dual Damascene/low-k integration problem [4].

Conclusion

It is clear that the integration of Copper metallization and low-k dielectrics must come to pass within the next two years if ITRS roadmap goals are to be achieved [5]. However, a series of very serious process integration issues must be resolved in regard to barrier materials, etch order, and the final character of the low-k ILD material before the integration of Copper metallization and ultra low-k dielectrics becomes a reality.

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NOTE: The Dual Damascene process sequences presented here have been greatly simplified for the purposes of this article. Detailed descriptions of these processing operations are presented in the course *Silicon Fabrication Technology* (a description of this course can be found in the "Educational Products" section of this web site).

References

[1] Steinbruchel, Christoph and Barry L. Chin; "*Copper Interconnect Technology*"; SPIE Press, 2001.

[2] Wolf, Stanley; "*Silicon Processing for the VLSI Era, Volume 4: Deep Submicron Process Technology*", Lattice Press, 2002.

[3]http://sst.pennnet.com/Articles/Article_Display.cfm?Section=Archives&Subsection=Display&ARTICLE_ID=137178

[4] http://sst.pennet.com/home.cfm

[5] http://public.itrs.net/files/2001itrs/home.htm