SPECIAL REPORT
SOI Wafer Technology for CMOS ICs

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Introduction:

SOI (**<u>S</u>**ilicon **<u>O</u>**n **<u>I</u>**nsulator) wafers have been used commercially as starting substrates for several decades in selected discrete and integrated circuit (IC) semiconductor device applications, particularly for use in extreme operating environments for military and space applications. The first SOI devices were developed for early satellite and space exploration systems in the 1960s. The key advantage of SOI wafers in these traditional applications was their resistance to ionization by radiation (e.g., solar wind radiation in space) and the robust voltage isolation of the IC.

Most of the early SOI devices were fabricated with SOS (**<u>S</u>**ilicon-**<u>O</u>**n-**<u>S</u>**apphire) wafers. The unique feature of today's SOI wafers is that they have a buried silicon oxide (**<u>B</u>**uried **<u>OX</u>**ide, or BOX) layer extending across the entire wafer, just below a surface layer of device-quality single-crystal silicon. The active elements (e.g., transistors in a CMOS IC) of semiconductor devices are fabricated in the single-crystal silicon surface layer over the BOX. The BOX layer provides robust vertical isolation from the substrate. Standard LOCOS (**<u>LOC</u>**al **<u>O</u>**xidation of **<u>S</u>**ilicon) or STI (**<u>S</u>**hallow **<u>T</u>**rench **<u>I</u>**solation) processes are employed to provide lateral isolation from adjacent devices.

At the present time, most SOI wafers are fabricated by use of one of two basic approaches. SOI wafers may be fabricated with the SIMOX™ (**<u>S</u>**eparation by **<u>IM</u>**planted **<u>OX</u>**ygen) process, which employs high dose ion implantation of oxygen and high temperature annealing to form the BOX layer in a bulk wafer [1,2,3]. Alternately, SOI wafers can be fabricated by bonding a device quality silicon wafer to another silicon wafer (the "handle" wafer) that has an oxide layer on its surface. The pair is then split apart, using a process that leaves a thin (relative to the thickness of the starting wafer), device-quality layer of single-crystal silicon on top of the oxide layer (which has now become the BOX) on the handle wafer. This is called the "layer transfer" technique, because it transfers a thin layer of device-quality silicon onto an oxide layer that was thermally grown on a handle wafer. The "layer transfer" approach has lead to the development of at least three production methods for fabrication of SOI wafers; SmartCut™ (UNIBOND) SOI wafers, NanoCleave™ SOI wafers, and ELTRAN™ SOI wafers [see reference 1 for description of these methods]. The SmartCut™ and NanoCleave™ processes both employ high dose ion implantation (using hydrogen or other light species), either alone or in combination with other steps,

to form a weakened silicon layer that splits (i.e., "peels off") the donor wafer, allowing the "layer transfer" to occur. The ELTRAN™ method (**E**pitaxial **L**ayer **TRAN**sfer) does not use ion implantation. It employs a layer of porous silicon, which is formed by anodic etching and annealing, to form the splitting layer.

Recently, there is strong interest in SOI wafers for application to the fabrication of advanced CMOS ICs. This is because SOI wafers provide a way to increase the speed performance of CMOS circuits, as well as reduce the power (and voltage) requirements to achieve high performance. The trade-off between performance and power dissipation is the most fundamentally challenging issue on the horizon for scaling of CMOS ICs. This issue threatens the roadmap of continuous scaling of CMOS devices. A solution must be found to insure the commercial dominance of CMOS ICs in the future, so it is little wonder that SOI, which offers solutions to this issue, is receiving serious attention at leading-edge companies developing advanced CMOS ICs. Compared to similar circuits fabricated on bulk silicon wafers, CMOS circuits fabricated on SOI wafers can run at 20-35% higher switching speeds than bulk CMOS, or 2 to 4 times lower power requirements when operating at the same speed as bulk CMOS [1,4]. These improvements in CMOS speed and power usage with SOI wafers are equivalent to 1-2 generations of scaling of CMOS devices on bulk silicon wafers.

SOI Advantages:

The SOI wafer structure has several important advantages over CZ bulk or epitaxial starting wafer architectures. SOI wafers potentially offer "perfect" transistor isolation (lower leakage), tighter transistor packing density (higher transistor count/higher IC function at the same lithographic resolution), reduced parasitic drain capacitance (faster circuit performance and lower power consumption), and simplified processing relative to bulk or epitaxial silicon wafers. Due to these advantages, SOI wafers appear ideal for leading edge integrated circuits with high speed, high transistor count, low voltage/low power operation, and battery operated systems requirements, such as portable logic or microprocessor ICs.

Silicon-on-insulator (SOI) wafers have traditionally been used for extreme environmental applications, such as high temperature and severe environments (e.g., outer space). However, they are expected to expand into mainstream CMOS applications due to these advantages:

- Excellent lateral and vertical isolation of active devices from substrate:
    - Elimination of inter-device leakage and latch-up in CMOS structures
    - Effective reduction of substrate coupling in RF circuits (allows higher quality inductors with increased Q factor)
    - Effective reduction of interference and cross-talk between devices in mixed-signal ICs

  - Reduced soft errors (e.g., in SRAM) from radiation effects (electron-hole pair generation)
  - Different voltages may be used on different devices without the added processing steps required for triple wells

- Faster device operation (speed/power product) due to reduction of parasitic capacitance (primarily due to reduced source-drain junction capacitance, but also from gate-to-substrate capacitance and metal-to-substrate capacitance):
  - IBM reported a 20% to 35% increase in chip speed for their PowerPC chips [4]

- Lower power consumption (speed/power product) due to lower operating voltages on devices and lower parasitic capacitance:
  - IBM reported a 35% to 70% reduction in power consumption for their PowerPC chips [4]

- More functions per die area or reduced die area per function; SOI allows tighter layout design rules (higher integration density), mainly due to reduced STI layout area required for lateral junction isolation (resulting from the absence of wells and the possibility of direct contact of the source-drain diodes in the NMOS and PMOS transistors) [4,5]

- Performance improvement equivalent to next technology node without scaling (e.g., performance of 0.25 micron devices on SOI wafers equivalent to performance of 0.18 micron devices on bulk wafers)

- Potential to simplify device fabrication steps:
  - Fewer masks and ion implantation steps, made possible by the elimination of well and field isolation implants
  - Less complex (costly) lithography and etching required to achieve next-generation performance

As noted above, SOI wafers offer the potential to simplify the process presently used for CMOS devices fabricated in bulk wafers. The process used for deep sub-micron CMOS on bulk wafers may be described in the following (highly simplified) way:

> 1) Formation of shallow trench isolation (STI) regions, which surround and define the active areas where transistors will be fabricated
>
> 2) Formation of deep n-type and p-type wells in the active areas, using high energy ion implantation; these wells are vertically "profiled" using multiple ion implantation steps to achieve:
>
> > 2a) A deep doping peak (the "deep well"), which suppresses latch-up, reduces soft errors (caused by charge pairs generated from

radiation effects), and which provides part of the ESD protection path
NOTE: if a deeper "triple well" (which is typically a deep n-well structure beneath and around a shallower p-well) is used for voltage isolation from substrate, it is formed just prior to formation of these n-type and p-type "twin wells"

2b) A shallower doping peak (the "field channel stop"), located just below the STI trench bottom, which suppresses lateral leakage between adjacent transistors within the wells (intra-well) and between adjacent transistors at the well boundaries (inter-well)

2c) A very shallow doping peak at the silicon surface (the "V_t adjust"), which sets the threshold voltage of the transistors

3) Formation of the gate stack, including the gate oxide insulator and the polysilicon gate on top of it (the polysilicon gate is highly doped, n-type for the n-channel transistors and p-type for the p-channel transistor); the gate electrode is subsequently defined by lithography and anisotropic etching.

4) Formation of the transistor body and contacts, including:

4a) Formation of source-drain extensions using ultra-low energy ion implantation (which is self-aligned to the gate electrode) and rapid thermal annealing (RTA)

4b) Formation of halo (punch-through stop) regions by self-aligned, high tilt implantation (and RTA)

4c) Following the formation of a sidewall spacer on the gate, formation of source-drain contact regions by high dose, low energy implantation (and RTA)

4d) Formation of salicide (**S**elf-**A**ligned si**LICIDE**) contact metal on the top of the gate and source-drain regions

The opportunity for fabrication process simplification mainly occurs in step 2 (specifically 2a and 2b), above. The use of SOI wafers eliminates the need for the high-energy ion implantation processes that form the deep n-type and p-type "twin" wells (step 2a) and field channel stop isolation regions (step 2b), which are presently required in leading edge bulk CMOS IC fabrication. Also, the formation of deep "triple well" structures using high energy ion implantation processes (see note in step 2a, above) is unnecessary with SOI wafers to achieve voltage (electrical) isolation from the substrate. Note that the ion implantation and RTA processes for the formation of transistors, e.g., extension and contact

source/drain formation (steps 4a and 4c), polysilicon gate doping (in step 3), and threshold voltage adjustment (step 2c) are still required with SOI wafers. However, it should be noted that ultra-shallow junction formation processes (steps 4a and 4c, above) could be less challenging in SOI wafers. In SOI wafers the ultra-shallow junction formation process may be designed so that the junction depth is determined by the silicon layer thickness, rather than the ion implantation and RTA processes. This results in a simplified process control challenge (e.g., it eliminates the impact of "transient enhanced diffusion" on final junction depth). Also, the requirement for the high tilt halo (punch through stop) ion implantation (step 4b) may be eliminated in "fully depleted" (FD) CMOS in SOI. [FD SOI CMOS will be defined later in this article.]

SOI Applications:

The application of SOI wafers to semiconductor devices may be segmented into three categories according to the thickness of the buried oxide (BOX) layer: thick, thin, and ultra-thin BOX layer wafers. The thin and ultra-thin BOX segments represent the highest growth potential segments for SOI wafers, because they can be used as starting wafers for CMOS IC fabrication. The table below summarizes the SOI wafer classification, the IC applications, and the key performance requirement. Note that the thickness boundaries delineating the thick, thin, and ultra-thin BOX classifications are somewhat arbitrary and not rigorously defined. Consequently, the values selected to delineate the thick, thin, and ultra-thin BOX categories will vary somewhat between different sources and will, to some degree, depend upon the perspective of the author.

The thickness of the device-quality, single-crystal silicon surface layer is also an important factor in the classification of SOI for applications. "Thick" SOI wafers, with silicon layers thicker than one micron (1000nm), are typically used for a wide variety of applications in power switching devices, high-speed bipolar circuits, and MEMS (**M**icro-**E**lectro-**M**echanical **S**ystems)[1]. At the moment, most commercial CMOS ICs are fabricated on SOI wafers with "thin" silicon surface layers (100-300nm), mainly using SIMOX™ or SmartCut™ SOI wafers, although ELTRAN™ SOI wafers are also being evaluated and qualified for use with commercial CMOS ICs. The trend in CMOS applications is clearly to thinner and thinner silicon surface layers. It is expected that commercial SOI CMOS fabrication will move from "thin" to "ultra-thin" silicon layers (30-100nm) in the near future (1-3 years) to support 0.1 micron CMOS fabrication. Furthermore, active industrial R&D is under way now at advanced IC companies on CMOS fabricated in "ultra-thin" silicon layers of 10-30nm, and there is conceptual and academic research activity on "nano-SOI" using layers less than 10nm.

SOI Wafer Classification, IC Applications, and Key Performance Requirements

SOI Wafer Classification (BOX)	BOX Thickness, Microns	System Level Application	IC Type	Key System Requirement
Ultra-thin	< 0.15	High End PCs	MPU	High Speed
Ultra-thin	< 0.15	Servers	MPU	High Speed
Thin	0.15 to 1	Workstation	ASIC – Logic	High Speed/Small Die
Thin	0.15 to 1	Handsets/PDA	Mixed Signal	Low Voltage/Power
Thin	0.15 to 1	Mainframes	High End Logic	High Speed
Thin	0.15 to 1	Portable "Wireless"	RF/IF trans/rec	Low Voltage/Power
Thin	0.15 to 1	Automotive	Mixed Signal	High Power
Thin	0.15 to 1	Consumer – Digital	ASIC – Logic	Low Voltage/Power
Thick	0.5 to 5	Military/Aerospace	RF/IF trans/rec	Radiation Hardened
Thick	0.5 to 5	Industrial	Bipolar, Power IC's	High Power

SOI Challenges and Issues:

The main barrier to the widespread adoption of SOI wafers for mainstream CMOS fabrication in the past has been the uncertain material quality and the higher cost of SOI wafers. However, these wafers are now demonstrating technical (materials quality) and economic (cost) readiness for use in mainstream CMOS IC production. The key materials quality issues are the continuity and thickness uniformity of the BOX and the defectivity and thickness uniformity of the device-quality, single-crystal silicon layer. Important BOX defects include voids and inclusions; the defects in the silicon top layer include threading dislocations and pits (COPs). Also, the interface charge trapped at the interface of the top silicon layer and the BOX must be kept small (less than ~$10^{11}/cm^2$). [The amount of charge at the BOX/silicon layer interface affects the electrical behavior of SOI CMOS transistors, e.g., threshold voltage and saturation current.] The suppliers of SOI wafers continue to aggressively improve materials quality and reduce cost, driven by the considerable economic motivation of a rapidly growing commercial market for SOI wafers and a clearly defined roadmap for SOI material quality on the ITRS Roadmap [8]. In this fast developing arena, reports of SOI materials quality measurements that are only a year old may be out of date.

Assuming that the issues of materials quality and cost will be adequately addressed, the adoption of SOI wafers for CMOS fabrication is a non-trivial task.

Fabricating CMOS devices in SOI presents challenges in device design and process integration, as well as in the process simulation, device simulation and circuit simulation TCAD tools. For example, dopant diffusion in the thin silicon layer over the BOX is dramatically altered in SOI by interaction of the diffusing dopants with the silicon/BOX interface (at the top of the BOX) [1]. This and other differences must be comprehended in process simulations and in process integration for IC fabrication. Adopting SOI wafers is not a simple transfer of a bulk CMOS device fabrication process into an SOI substrate.

There are also significant differences between the way a bulk or epitaxial silicon CMOS device and an SOI CMOS device behave electrically. For example, “short channel effects” (SCE) are typically suppressed more effectively in SOI CMOS devices than in bulk CMOS, and SOI CMOS devices typically have lower subthreshold leakage (“off current”) and higher saturation current (“on current”) than bulk CMOS counterparts [5]. Consequently, the SOI CMOS circuits typically demonstrate higher speed performance and lower power dissipation than bulk or epitaxial CMOS. Also, the SOI CMOS device exhibits several parasitic phenomena that are not typically observed in the bulk or epitaxial CMOS device [5,6]. These phenomena are related to impact ionization in the high electric field that occurs near the drain in CMOS devices, and the fact that the channel terminal in the SOI CMOS device is isolated from the substrate, unless specific measures, such as body ties [6], are explicitly employed. In other words, the body of the SOI device is “floating”. There are several anomalous electrical behaviors in SOI CMOS devices that arise from these “floating body effects” (such as a “kink” in the output I-V characteristic of the SOI CMOS device and degraded drain breakdown voltage). Note that floating body effects are not necessarily all bad, as they may be employed to increase the current output from an SOI CMOS device [6]. The point is that the SOI CMOS transistor is different than the bulk CMOS transistor and these differences must be reflected in the simulators employed to design devices and circuits for CMOS ICs fabricated in SOI wafers.

SOI CMOS transistors also exhibit so-called self-heating effects [5,6]. These effects arise in SOI devices because the device is thermally insulated from the substrate by the buried oxide (BOX). Consequently, removal of excess heat generated within the device by device switching is not removed as efficiently in SOI devices as it is in bulk devices. This leads to a substantial elevation of temperature within the SOI device (50-150^{0}C). This modifies the output I-V characteristics of SOI devices, once sufficient power has been dissipated within the devices. Note that this self-heating effect only appears when power is being dissipated within the device (that is, when the transistor is on, conducting current through its channel). This only occurs in CMOS circuits when a logic stage is switching state, not when it is in a stand-by state (e.g., holding a logic high or low state).

These effects certainly will not prevent the widespread adoption of SOI for CMOS ICs, but they must be taken into account by thoughtful device and circuit design approaches that specifically address the peculiarities of the SOI CMOS transistor vs. the bulk or epitaxial wafer CMOS transistor. Obviously, the process simulation, device simulation, circuit simulation, and layout TCAD tools employed by designers must accurately model the peculiarities (and advantages) of SOI CMOS to achieve optimal device design, circuit design, layout and processing approaches for CMOS ICs fabricated with SOI wafers.

CMOS transistors designed for use with SOI wafers are classified by the thickness of the device-quality single-crystal silicon layer (at the surface above the BOX) relative to the depths of the source-drain junction and channel depletion layers in the device with the operating voltages applied. An SOI CMOS transistor is classified as "partially depleted" (PD) if the silicon surface layer is thicker than the depth of the depletion region in the transistor's channel. The SOI CMOS transistor is classified as "fully depleted" (FD) if the silicon surface layer is equal to the depth of the depletion region in the transistor's channel. The transistor will be partially depleted or fully depleted depending on the silicon layer thickness above the BOX and the doping concentration in the channel. To form a fully depleted SOI transistor, the channel doping concentration must be low enough that the gate depletion region extends throughout the entire thickness of the silicon layer. When the silicon surface layer is thicker than about 200nm, the transistor will typically be partially depleted, unless the channel doping concentration is reduced to such low values that the threshold voltage is too low for practical CMOS applications (less than 100mV) [5]. If the silicon layer thickness is reduced to about 100nm, the transistor will be fully depleted, even when the channel doping concentration is increased to produce threshold voltages of 300-400mV. If the silicon layer thickness is reduced further (70nm), the transistor will remain fully depleted even if the channel doping concentration is increased to produce even higher threshold voltages (700mV).

There are significant differences in partially depleted and fully depleted SOI CMOS transistors [5]. For example, the threshold voltage of the fully depleted (FD) device is very sensitive to the silicon surface film thickness. This results in an addition source of manufacturing variance in the fabrication of FD SOI CMOS. Typically, this is on the order of 10mV in threshold voltage per nanometer of variation in the silicon film over the BOX. This is the main reason why, at the present time, the fabrication of commercial CMOS on SOI typically employs partially depleted (PD) devices. However, careful device design and optimizing the channel implant process can reduce this sensitivity in FD devices. It is also important to note that the variation of drain (saturation) current does not have the same sensitivity to film thickness as the threshold voltage in FD SOI CMOS [5].

There are significant advantages for FD transistors over PD transistors, and the trend in SOI CMOS is toward the use of fully depleted devices. A fundamentally important point is that in FD SOI CMOS the subthreshold slope can be very low (less than ~65 mV/decade (i.e., a 65 mV increase in gate voltage will result in a tenfold increase in the subthreshold drain current). This is significantly closer to the theoretical minimum (~60 mV/decade) than the typical values of 80-85 mV/decade in PD SOI CMOS and 85-90 mV/decade (best case) in bulk CMOS. This is a critical advantage. It allows the threshold voltage of the FD SOI CMOS device to be very low (150-200mV) with acceptable subthreshold leakage ("off current"), which determines off-state power dissipation. Lowering the threshold voltage also means that the supply voltage can be reduced significantly without degrading CMOS IC speed performance (the supply voltage needs to be 4-5 times the threshold voltage; below this ratio, the speed performance of the circuit will degrade rapidly). The reduction of the supply voltage produces a significant reduction in active (switching) power dissipation, without unacceptable performance degradation. [Note: the active power dissipation is also reduced somewhat by reduction of parasitic capacitance in SOI CMOS relative to bulk CMOS.] Also, in the FD CMOS device the variation of threshold voltage with temperature is significantly less (2-3 times less) than in the PD CMOS device. Furthermore, in general, the anomalous electrical behaviors arising from floating body effects in SOI CMOS transistors are less of a problem in FD transistors than they are in PD transistors. Consequently, it is expected that FD SOI CMOS transistors will be generally adopted in the near future [1]. Converting an existing PD SOI CMOS device and circuit design into FD CMOS is expected to be straightforward [6], at least in comparison with to the challenges in the conversion from bulk CMOS to SOI CMOS.

SOI Prospects:

SOI wafers are now viewed as the most important emerging wafer engineering technology for use in leading edge CMOS IC production during the next 3-5 years. One plausible scenario during this period is the rapid adoption of SOI wafers in place of epitaxial silicon wafers now employed as starting substrates for high-end logic device (e.g., microprocessors) and SOC (**S**ystem **O**n **C**hip) applications at the 0.13 and 0.10 micron technology nodes. SOI wafers appear to offer an excellent platform for integrating RF and digital circuits on the same chip.

Major semiconductor market research firms have forecasted the possibility that SOI wafers may make up 10% of all silicon wafers used by 2010. Almost all of the "top 20" chipmakers have publicly expressed high interest in the inherent advantages of SOI wafers (e.g., IBM, Intel, AMD, etc.). A bright spotlight was cast on SOI wafer technology production in August 1998 due to an IBM announcement that they would adopt SOI wafer technology using the SIMOX SOI wafer process in high volume manufacturing on leading edge

microprocessor architecture. It is in production now, using a partially depleted transistor architecture [4]. Furthermore, Intel has recently unveiled their vision of the CMOS device they will pursue in the future, to achieve continuous scaling of CMOS with high performance and acceptable power (and voltage) requirements. This is the Intel "TeraHertz Transistor", which employs the use of a fully depleted (FD) CMOS transistor on thin SOI wafers [7], among other design changes (such as a high-K gate dielectric and raised source-drain regions).

One of the more compelling reasons why support for migration from bulk to SOI CMOS is growing is due to the problems created by the exponential growth of the power dissipated by high performance, high density CMOS ICs in bulk (or epitaxial) silicon as scaling has been pursued [7]. For example, as Intel microprocessors have evolved by scaling through the 286, 386, and 486 generations into and through the Pentium generations, power dissipation has dramatically (exponentially) increased. The 286 generation ran warm (to the touch by your fingers), the 386 ran very hot, and the 486 ran so hot that it needed a small fan to cool it. As evolution proceeded through the Pentium generations, the cooling requirement was more demanding at each generation, using more powerful fans and adding cooling fins to the microprocessor package to improve heat transfer out of the IC. Assuming that the Intel microprocessor stays on its historical trend lines (Moore's Law), then by about 2005 these ICs will have about 1 billion transistors and operate at about 10 GigaHertz [7]. They will also dissipate so much power that they would require cooling by refrigeration of a liquid coolant in good thermal contact with the IC package. This is unacceptable as a computer systems requirement, and it illustrates that power dissipation is becoming a major barrier to scaling high performance, high density CMOS in the very near future. SOI CMOS offers a way to avoid this barrier without sacrificing high performance or high density.

SOI devices also appear to offer a sustainable, long-term pathway beyond the multiple barriers to scaling planar, bulk CMOS to 50nm and below [1]. If the present understanding of the barriers and problems to scaling planar, bulk CMOS below 50nm is correct, then it is expected that a dramatic shift to fully-depleted SOI CMOS will occur in the 2006-2008 timeframe. If the many challenges in the fabrication of "ultra-thin" SOI wafers are met (adequate materials quality and acceptable cost), and if device design and lithography challenges are met, the way to 25nm CMOS is open, enabled in part by SOI substrates.

SOI wafers will have a very significant impact on both the IC fabrication process and process equipment. For example, SOI wafers create a requirement for new types of ion implantation process equipment. Most SOI wafers are fabricated using an ion implantation step employing a high dose of oxygen (Ibis' SIMOX™ SOI wafer process) or hydrogen (SOITEC's SmartCut™ SOI wafer process). These process requirements create a requirement for two new types of

specialized ion implantation machines: a high dose oxygen implanter, and a high dose hydrogen implanter.

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NOTE: Robert Simonton is developing a new course on SOI that will describe these topics in far more technical detail than is provided here in this special report. Keep an eye on this website for more information on the content and availability of this new course.

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