

Properties of Silicon

Written by: Scotten W. Jones

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Preface

The following document was written in 2000 as a chapter on Properties of Silicon for inclusion in a highly technical - text book on Silicon Integrated Circuit Process Technology. For marketing reasons we abandoned the book without completing it but this was one of several chapters that are complete. This chapter is a follow on to a chapter on diffusion we posted previously. We hope you find it useful.

Please note that this material was written back when we planned to publish it as a hard cover book in black and white and is not in color the way all of the current IC Knowledge reports are.

Scotten W Jones
President
IC Knowledge LLC
January 2, 2008

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1 Properties of Silicon

- 1.1. Introduction
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1.1. Introduction

Silicon is the dominant material for integrated circuit (IC) fabrication. In this chapter the properties of silicon will be reviewed with a particular emphasis on silicon properties relevant to subjects presented later in the book. The chapter opens with basic silicon structure and mechanical properties and then proceeds to the intrinsic electrical properties, the subject of doping will be presented followed by the extrinsic (doped) electrical properties of silicon, point and extended defects will be discussed and finally the preparation and properties of commercial silicon will be reviewed.

1.2. Crystal structure and mechanical properties

Silicon has an atomic number of fourteen. In isolation a silicon atom in the ground state has the electron configuration given in table 1.1. The 1s, 2s, 2p, and 3s energy levels are all filled and the 3p energy level has 2 electrons occupying levels with a capacity of 6 electrons. In the solid state - silicon satisfies the unfilled 3p energy levels by sharing electrons with the four nearest neighbor atoms forming covalent bonds - see figure 1.1.

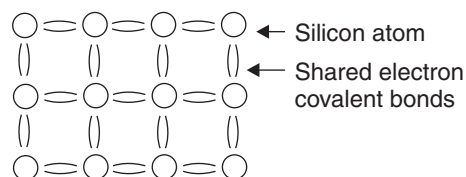


Figure 1.1: Silicon covalent bonds.

Table 1.1: Silicon ground state energy levels.

n	l	m_l	m_s	Shell	Subshell	# of allowed states	# of occupied states
1	0	----	$\pm 1/2$	K	1s	2	2
2	0	0	$\pm 1/2$	L	2s	2	2
	1	-1,0,1	$\pm 1/2$	L	2p	6	6
3	0	0	$\pm 1/2$	M	3s	2	2
	1	-1,0,1	$\pm 1/2$	M	3p	6	2
	2	-2,-1,0,1,2	$\pm 1/2$	M	3d	10	0

In the crystalline phase silicon forms a diamond structure. The construction of a silicon unit cell is illustrated in figure 1.2

The silicon diamond unit cell can be visualized by starting with a simple cubic cell with corner atoms - figure 1.2a (corner atoms are shaded gray). Add the six face centered atoms - figure 1.2b (additional face atoms shaded gray). Add an atom at $1/4, 1/4, 1/4$ from each face and corner atom, - figure 1.2c (added atoms shaded gray). Note that only the atoms that actually fall inside the unit cell are added. Figure 1.2d illustrates the final unit cell with atomic bonds. Figure 1.2e illustrates a single silicon tetrahedra illustrating the four nearest neighbor bonds.

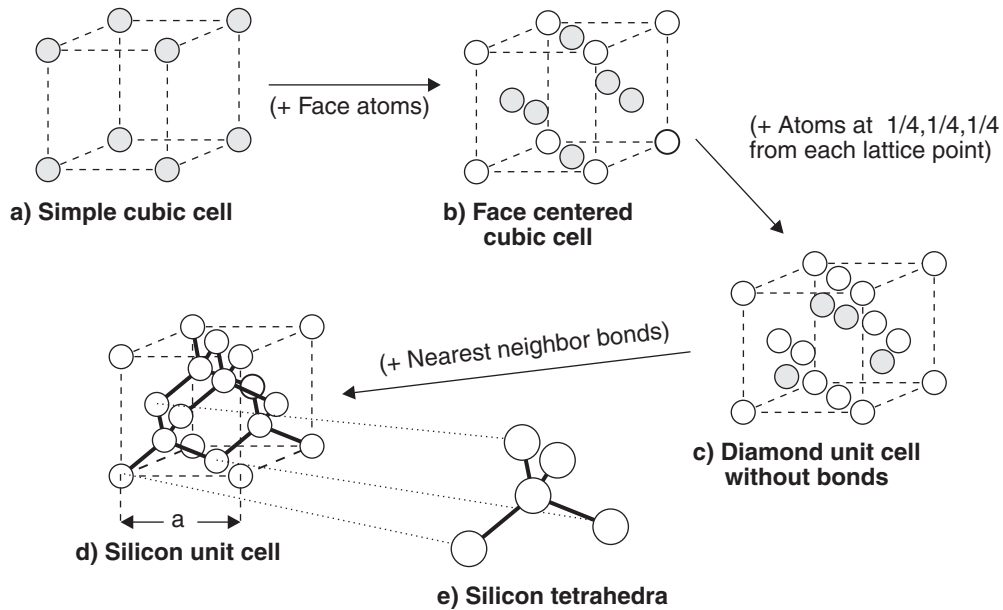


Figure 1.2: Construction of the silicon unit cell.

The unit cell shown in figure 1.2 is repeated throughout the crystal structure of solid silicon.

The lattice constant a , for silicon is 0.543nm or 5.43×10^{-8} cm (see figure 1.2d to define a). The silicon unit cell contains 8 atoms - $8 \times 1/8$ corner atoms, $6 \times 1/2$ face atoms, and 4 atoms at $1/4, 1/4, 1/4$, lattice points. The unit cell volume is therefore 1.6×10^{-22} cm³, which gives 6.25×10^{21} unit cells/cm³, and 5.00×10^{22} silicon atoms/cm³. The nearest neighbor distance is 0.235nm. Silicon atoms have a covalent radius of 0.118nm so if the atoms are considered hard spheres the unit cell-packing ratio is 27%.

1.2.1. Miller indices

Crystal planes within a solid are specified by Miller indices. Miller indices utilize a set of three numbers to indicate the crystal plane relative to the x , y and, z direction. Figure 1.3 defines the Miller indices for common silicon crystal planes.

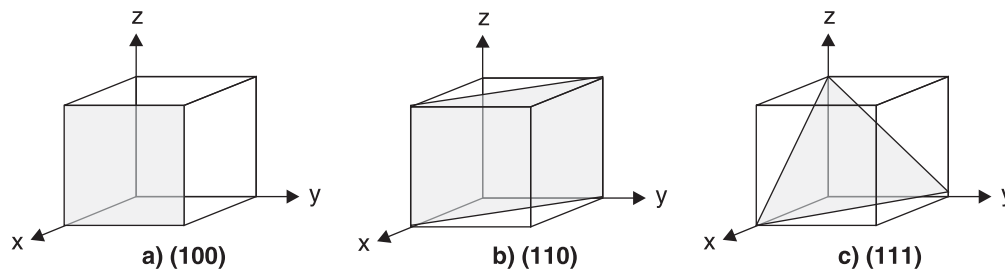


Figure 1.3: Miller indices of selected planes for a cubic crystal.

Silicon substrates utilized to fabricate integrated circuits are oriented along one of the crystal planes defined in figure 1.3. The (111) crystal plane (figure 1.3c) is the least expensive substrate orientation to produce and is used to fabricate bipolar devices. Substrates oriented on the (110) crystal plane are difficult to produce and are only used for experimental purpose (figure 1.3b). Substrates oriented on the (100) crystal plane have the best surface properties and are widely used to produce MOS integrated circuits - the dominant IC technology (figure 1.3a).

1.2.2. The (100), (111) and (110) silicon surfaces

Termination of the silicon lattice at the surface leaves unfilled energy states and exposed surfaces bonds that have processing and electrical consequences. The following is a brief discussion of each silicon surface.

1.2.2.1. The (100) surface

The (100) surface has a unit cell area - see figure 1.4a

$$A = a^2 \quad (1.1)$$

where a is the lattice constant. The unit cell area is therefore 2.95×10^{-15} cm² and each unit cell contains 2 atoms yielding 3.39×10^{14} cells/cm² and 6.78×10^{14} atoms/cm². There are 4 dangling surface bonds per unit cell or 1.36×10^{15} bonds/cm².

1.2.2.2. The (110) surface

The (110) surface has a unit cell area - see figure 1.4b

$$A = a^2 \sqrt{2} \quad (1.2)$$

The unit cell area is $4.17 \times 10^{-15}/\text{cm}^2$ and each unit cell contains 4 atoms yielding 2.40×10^{14} cells/ cm^2 and 9.60×10^{14} atoms/ cm^2 . There are 8 surface bonds (dangling plus parallel) per unit cell [1] or 1.92×10^{15} bonds/ cm^2 .

1.2.2.3. The (111) surface

The (111) surface has a unit cell area - see figure 1.4c

$$A = \frac{1}{2} a^2 \sqrt{3} \quad (1.3)$$

The unit cell area is $2.55 \times 10^{-15}/\text{cm}^2$ and each unit cell contains 2 atoms yielding 3.92×10^{14} cells/ cm^2 and 7.83×10^{14} atoms/ cm^2 . There are 4 surface bonds per unit cell [1] or 1.57×10^{15} bonds/ cm^2 .

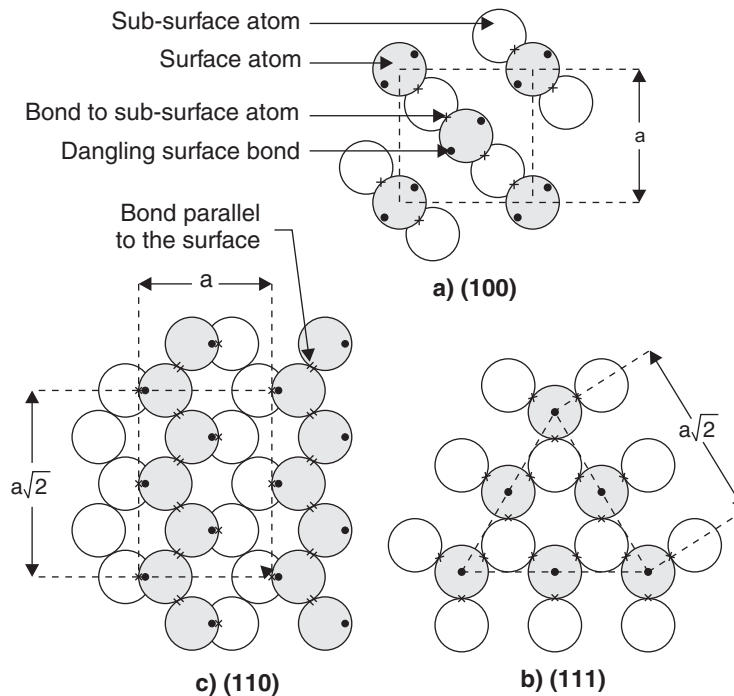


Figure 1.4: Silicon (100), (110), and (111) surfaces.
Adapted from [1].

1.2.3. Physical properties of silicon

Table 1.2 summarizes some selected physical properties of silicon. Appendix D contains a more extensive compilation of silicon properties.

Table 1.2: Selected physical properties of silicon

Property	Value	Units
Symbol	Si	
Atomic density	4.995×10^{22}	atoms/cm ³
Covalent radius	0.188	nm
Density of surface atoms		
(100)	6.78×10^{14}	atoms/cm ²
(110)	9.59×10^{14}	atoms/cm ²
(111)	7.83×10^{14}	atoms/cm ²
Lattice constant	0.543	nm
Nearest neighbor distance	0.235	nm

1.3. Intrinsic electrical properties

The close proximity of silicon atoms in the solid-state leads to overlap in the allowed energy levels and causes a splitting of each level into the allowed states multiplied by N, where N is the number of atoms in the solid - see figure 1.5. The outer most energy levels form two bands referred to as the valence band and the conduction band. At zero degrees Kelvin the valence band is completely filled with electrons and the conduction band is completely empty of electrons. A forbidden energy gap separates the conduction band from the valence band.

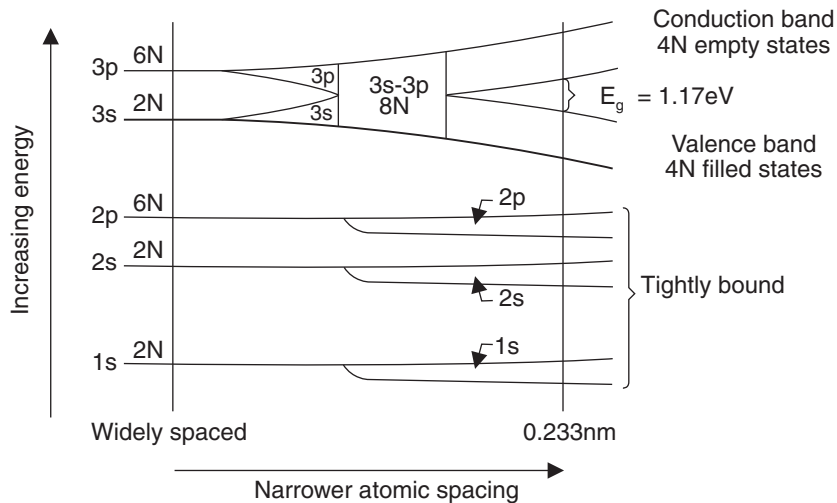


Figure 1.5: Silicon band structure at 300K.

1.3.1. Energy gap

The energy gap separates the conduction and valence bands with an area that contains no allowed energy states. For an electron in the valence band to reach the conduction band and become mobile, the electron must overcome the energy gap. The height of the energy gap is characteristic of the materials electrical properties. Semiconductors such as silicon have energy gaps of 0.1 - 2.0 electron volts (eV), insulators have energy gaps of several eV, and conductors have overlapping valence and conduction bands. The relatively large energy gap in insulators requires a great deal of energy to cause conduction, whereas metals have no gap and require very little energy to cause conduction, semiconductors require an amount of energy intermediate between an insulator and a conductor. The height of the energy gap for silicon depends on temperature and is given by [2]

$$E_g(T) = 1.17 - \frac{4.73 \times 10^{-4} T^2}{636 + T} \quad (1.4)$$

where T is the temperature in degrees Kelvin and 1.17 is the silicon energy gap at zero degrees Kelvin.

Figure 1.6 illustrates the silicon energy gap versus temperature calculated from (1.4)

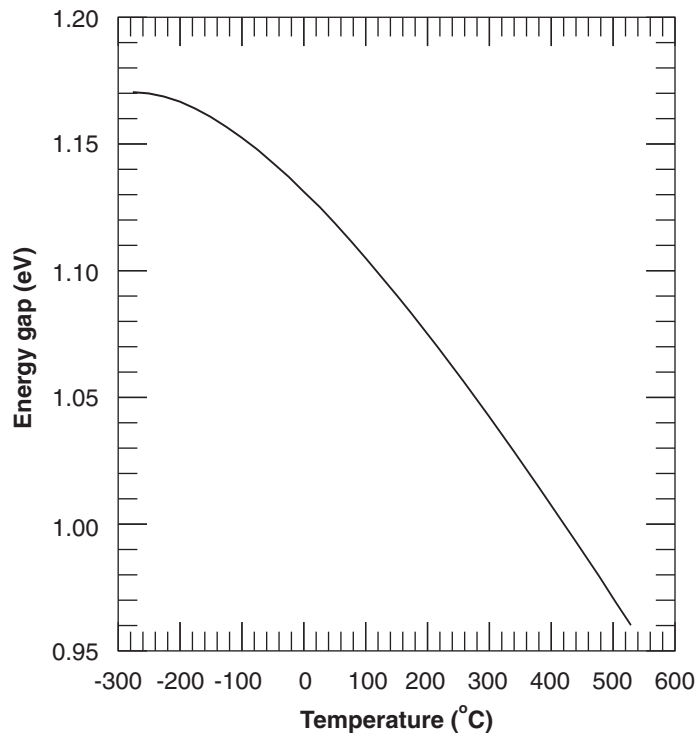


Figure 1.6: Silicon energy gap versus temperature.

1.3.2. Intrinsic carrier concentration

As the silicon temperature is raised above zero degrees Kelvin, there exists a finite probability that an electron excited by thermal energy will jump from the valence band to the conduction band and become a mobile carrier. Electrons that have jumped to the conduction band are called intrinsic carriers and the intrinsic carrier concentration versus temperature is given by [3]

$$n_i = 3.10 \times 10^{16} T^{3/2} e^{-1.206/kT} \quad (1.5)$$

where k is Boltzmann's constant.

Figure 1.7 illustrates the silicon intrinsic carrier concentration versus temperature calculated from (1.5)

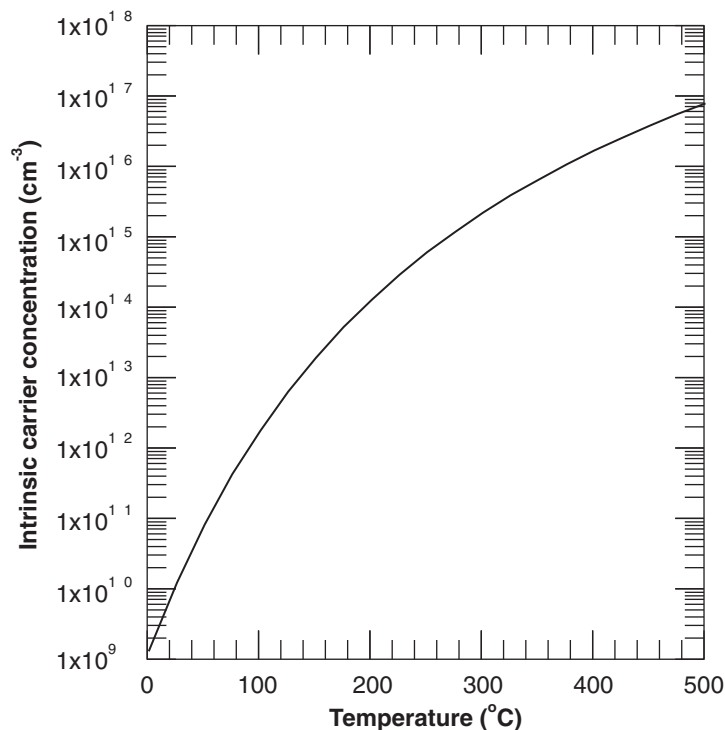


Figure 1.7: Silicon intrinsic carrier concentration versus temperature.

1.4. Doping

The introduction of impurities into silicon is referred to as doping and allows the electrical properties of silicon to be altered. Consider the section of the periodic table illustrated in figure 1.8.

The group IV elements are all semiconductors including silicon. The group V elements each have one more electron than silicon in the outer most energy level. Introducing group V impurities into silicon adds a filled electron energy level to the silicon forbidden gap near the

conduction band, these atoms are referred to as donors. The added electron is easily ionized into the conduction band where it is free to move about the silicon lattice. Introducing group III impurities into silicon adds an unfilled energy level to the forbidden gap near the valence band and these atoms are referred to as acceptors. The unfilled energy level is easily ionized by capturing an electron from the valence band. The electron ionized from the valence band leaves behind a “hole” that is free to move through the valence band and acts as a positive charge carrier of equal but opposite charge type to an electron (see figure 1.9).

III	IV	V
5 B	6 C	
13 Al	14 Si	15 P
31 Ga	32 Ge	33 As
49 In	50 Sn	51 Sb

↑ Acceptors ↑ Semiconductors ↑ Donors

Figure 1.8: Periodic table section.

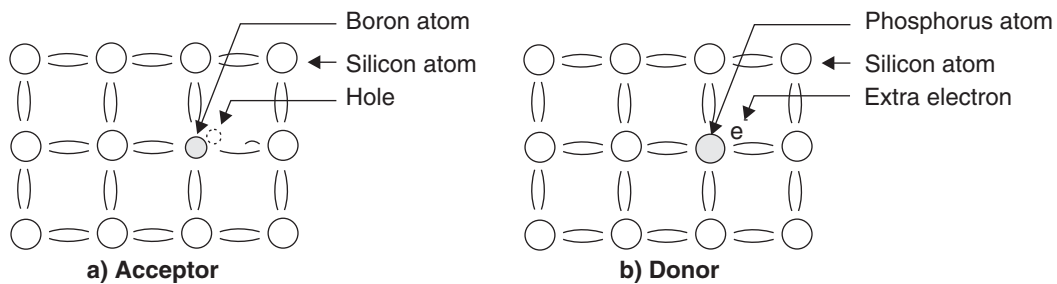


Figure 1.9: Dopants in silicon.

Figure 1.9a illustrates a group III impurity added to silicon - boron, and figure 1.9b illustrates a group V impurity added to silicon - phosphorus. Boron and phosphorus were chosen for the illustration because they are two of the most common silicon dopants. The action of other group III and V dopants is similar to boron and phosphorus respectively.

Figure 1.10 illustrates the energy levels introduced into the silicon energy gap for a variety of impurities [4],[5],[6],[7].

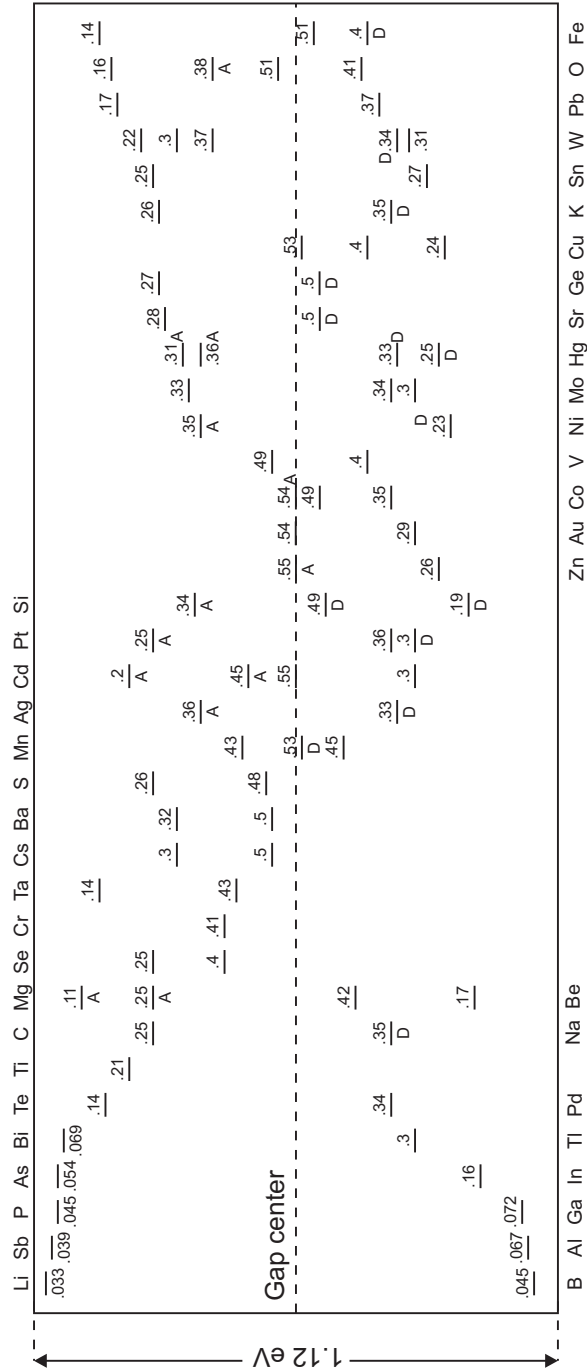


Figure 1.10: Ionization energy of impurities in silicon [4],[5],[6],[7].

1.5. Extrinsic electrical properties

When the concentration of carriers introduced into silicon by doping exceeds the intrinsic carrier concentration, the silicon is said to be extrinsic. In this section the properties of extrinsic silicon will be reviewed.

1.5.1. n and p type silicon

If silicon is doped with a group III impurity to a concentration in excess of the intrinsic carrier concentration, then the doped silicon will have an excess of mobile positive carriers (holes). Silicon with excess positive carriers is referred to as p-type. If silicon is doped with a group V impurity to a concentration in excess of the intrinsic carrier concentration, then the doped silicon will have excess negative carriers. Silicon with excess negative carriers is referred to as n-type.

- p-type - silicon with a mobile positive carrier concentration higher than the intrinsic carrier concentration.
- n-type - silicon with a mobile negative carrier concentration higher than the intrinsic carrier concentration.

The type of carrier - positive or negative, in the majority in an area of doped silicon is referred to as the majority carrier. Even in highly doped silicon some carriers of type opposite to the carrier type introduced by the dopant exist due to ionization. The lower concentration carrier in a doped region is referred to as the minority carrier.

1.5.2. Mobility

At room temperature the carriers introduced by doping are mostly ionized and free to move through the silicon lattice. The rate at which the carriers move under the influence of an electric field is called the mobility. For low electric fields the drift velocity is related to the electric field by the mobility as

$$v_d = \mu E \quad (1.6)$$

where, v_d is the drift velocity, μ is the mobility and E is the electric field.

Ionized impurities and acoustic phonon scattering limit mobility in silicon.

The NIST formula for mobility versus phosphorus doping is given by [8]

$$\text{Log}_{10}(\mu/\mu_0) = \frac{a_0 + a_1x + a_2x^2 + a_3x^3}{1 + b_1x + b_2x^2 + b_3x^3} \quad (1.7)$$

and

$$\mu_0 = 1 \frac{cm^2}{V \cdot s} \quad (1.8)$$

$$n_0 = 1 \times 10^{16}/cm^2 \quad (1.9)$$

$$x = \log_{10}(n/n_0) \quad (1.10)$$

where n is the carrier concentration and at 23°C the constants are:

$$\begin{aligned} a_0 &= 3.0746 \pm 0.0025 \\ a_1 &= -2.2679 \pm 0.0076 \\ a_2 &= 0.62998 \pm 0.00245 \\ a_3 &= -0.061285 \pm 0.00087 \\ b_1 &= -0.70017 \pm 0.00290 \\ b_2 &= 0.19839 \pm 0.00113 \\ b_3 &= -0.020150 \pm 0.00041 \end{aligned}$$

There is no corresponding NIST formula for hole mobility. A formula developed by Antoniadis, et.al. that fits well to experimental data is given by [9].

$$\mu = \frac{468 - 49.7}{1 + (n/1.6 \times 10^{17})^{0.7}} + 49.7 \quad (1.11)$$

Figure 1.11 presents mobility versus doping for boron and phosphorus doped silicon calculated from (1.7) and (1.11).

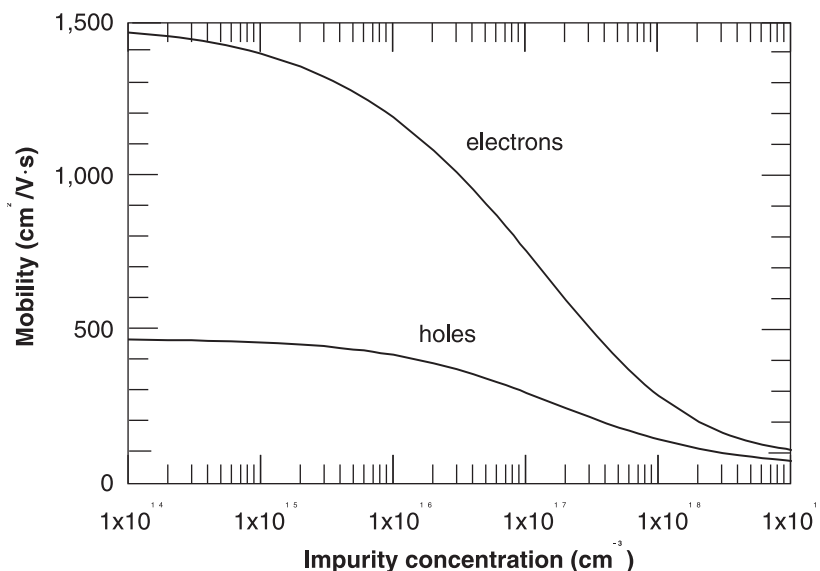


Figure 1.11: Carrier mobility in boron and phosphorus doped silicon.

As can be seen from figure 1.11, electrons have a much higher mobility in silicon than holes. The differences in mobility for holes versus electrons leads to differences in performance for devices that rely on electrons such as NMOS transistors versus the performance of devices

that rely on holes such as PMOS transistors. For example, PMOS devices have to be made larger than NMOS devices for the same drive current.

1.5.3. Resistivity

Resistivity is a fundamental electrical property of a material with the resistance of a uniform bar of material given by

$$R = \frac{\rho L}{A} \quad (1.12)$$

where ρ is the resistivity, L is the length of the bar, A is the cross sectional area of the bar, and R is the resistance of the bar.

For a doped semiconductor the resistivity is given by

$$\rho = \frac{1}{nq\mu(n)} \quad (1.13)$$

where n is the carrier concentration and q is the carrier charge (equal to the charge on the electron).

From (1.13) and either (1.7) or (1.11) - whichever is appropriate for the carrier type of interest, the resistivity of a uniformly doped semiconductor material may be determined (see figure 1.12).

1.5.4. Fermi level

The Fermi level is the energy at which the probability of occupancy of an energy state by an electron is one half. For intrinsic silicon the Fermi level is located at approximately the center of the forbidden energy gap. The position of the Fermi level relative to the top of the valence band versus temperature for intrinsic silicon is given by [4]

$$E_F = \frac{E_C + E_V}{2} + \frac{3kT}{4} \ln \left(\frac{m_{dh}}{m_{de} M_c^{2/3}} \right) \quad (1.14)$$

where: $m_{dh} = 1.9117$, $m_{de} = 0.3286$ and M_c is the number of equivalent minima in the conduction band [10].

For extrinsic silicon where n or $p \gg n_i$, the Fermi level for n-type silicon is given by

$$E_F - E_i = kT \ln \left(\frac{n}{n_i} \right) \quad (1.15)$$

and for p type silicon by

$$E_F - E_i = kT \ln \left(\frac{p}{n_i} \right) \quad (1.16)$$

where n and p are the doping concentration for n-type and p-type silicon respectively and E_i is the intrinsic Fermi level.

The Fermi level versus temperature and doping is presented in figure 1.13.

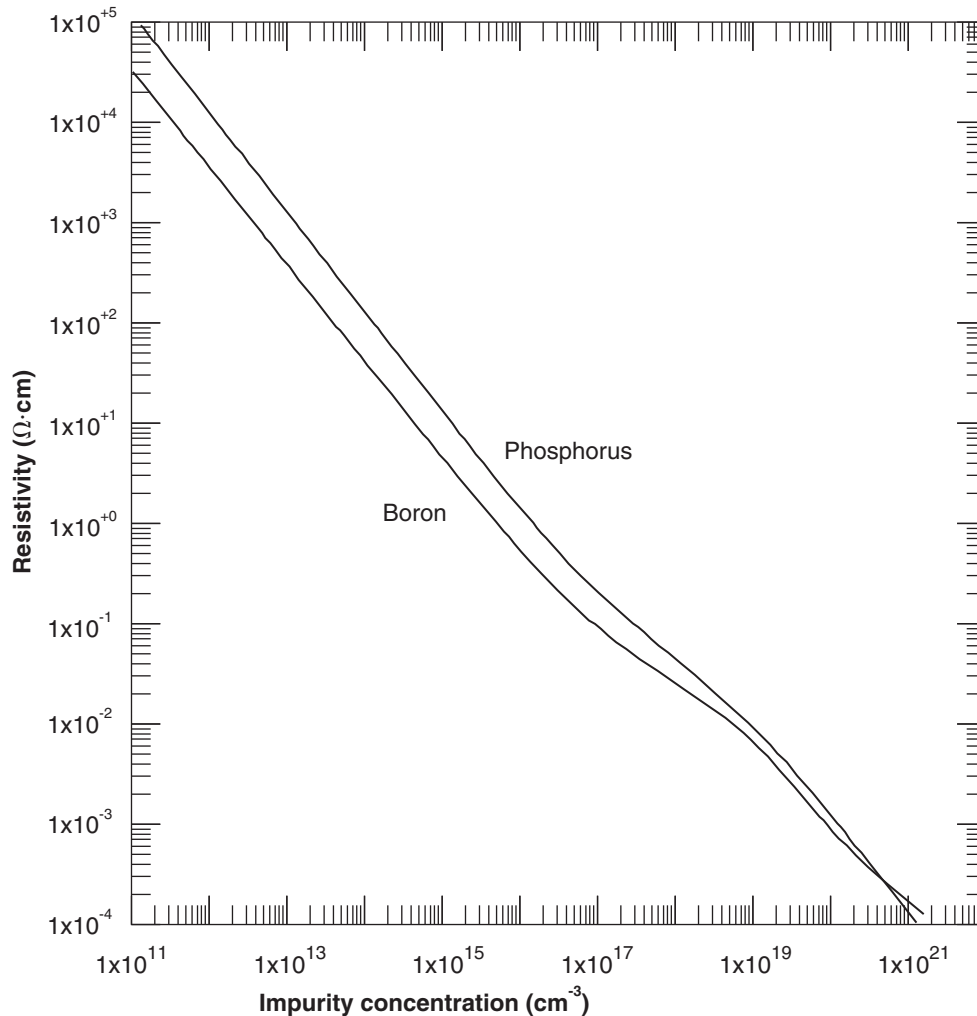


Figure 1.12: Resistivity of silicon versus doping concentration at 300°K.

1.6. Point and extended defects

Point defects in silicon play an important role in impurity diffusion and extended defect formation. Extended defects can create electrical leakage paths degrading the performance of semiconductor devices. In this sections the properties of point and extended defects will be discussed.

1.6.1. Point defects

There are two major types of point defects, vacancies and interstitials.

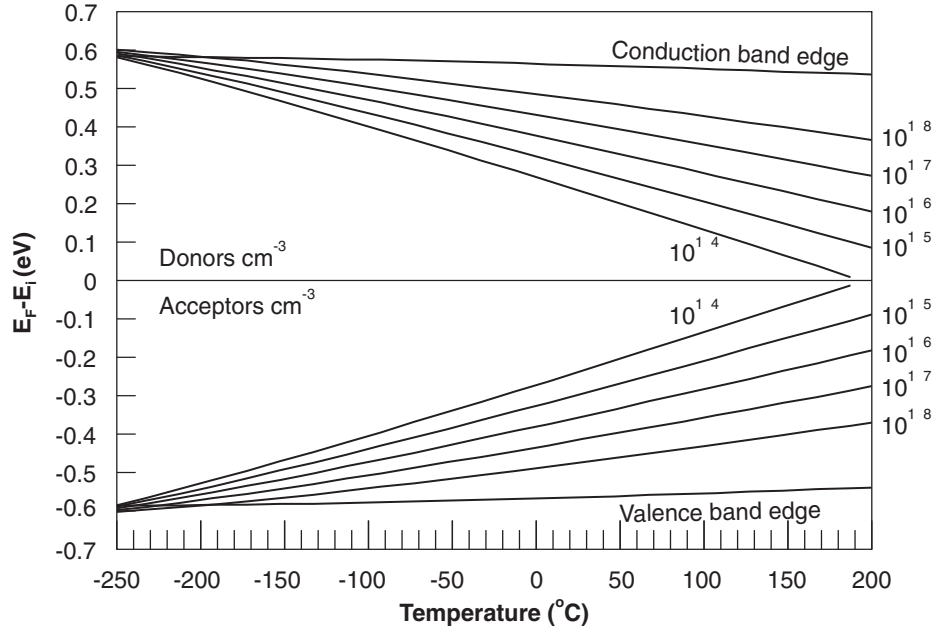


Figure 1.13: Fermi level versus temperature and doping.

1.6.1.1. Vacancies

Vacancies are silicon atoms missing from the silicon lattice. Figure 1.14a illustrates a silicon tetrahedra, figure 1.14b illustrates a simple vacancy - one silicon atom missing, and figure 1.14c illustrates a divacancy - two silicon atoms missing.

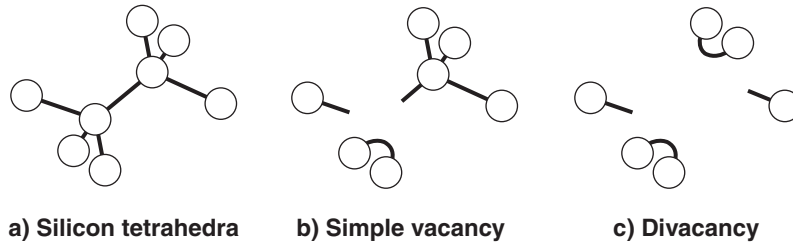


Figure 1.14: Silicon vacancy defects.

1.6.1.2. Interstitials

Interstitials are atoms located at non-lattice positions. Figure 1.15a illustrates a simple interstitial, 1.15b illustrates a bond-centered interstitial and 1.15c illustrates a split (100) interstitial.

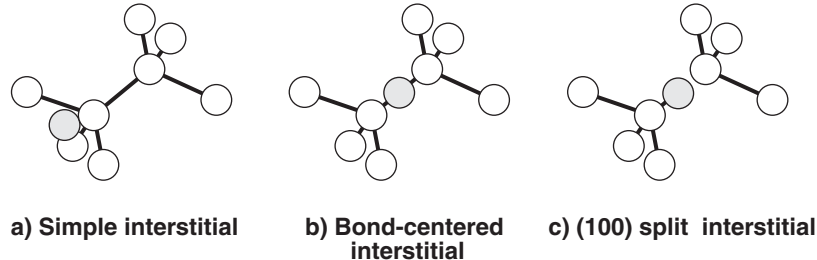


Figure 1.15: Silicon interstitial.

In the silicon unit cell there are 5 interstitial positions $(1/2, 1/2, 1/2)$, $(1/4, 1/4, 1/4)$, $(1/4, 3/4, 3/4)$, $(3/4, 1/4, 3/4)$, and $(3/4, 3/4, 1/4)$.

1.6.1.3. Point defect concentrations

There are three mechanisms for the formation of point defects.

1. Schottky defect - a silicon atom jumps to an interstitial position and diffuses to a surface leaving the lattice and creating a vacancy without a matching interstitial - see figure 1.16a.
2. Frenkel defect - a silicon atom jumps to an interstitial position creating a vacancy interstitial pair - see figure 1.16b.
3. Surface generation - surface atoms move to interstitial sites within the lattice - see figure 1.16c.

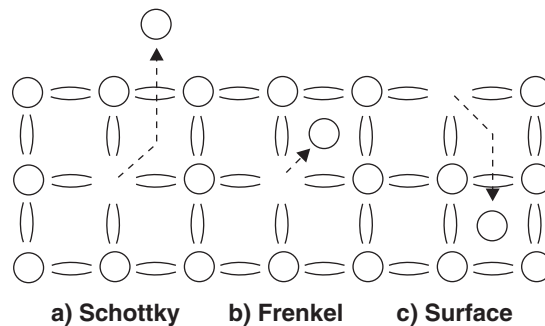


Figure 1.16: Point defect generation mechanisms.

The point defect concentration in a crystalline material depends on thermal fluctuations and vapor pressure. For silicon the vapor pressure is so low over the temperatures of interest that only thermal fluctuations are important. The presence of defects changes the internal energy of the crystal and the entropy, therefore the equilibrium concentration of defects should depend on the energy of formation and the equilibrium temperature. Gandhi derives the concentration of Schottky and Frenkel defects as follows [11]

1.6.1.3.1. Schottky defect concentration

Assume only Schottky defects occur. The number of ways in which a Schottky defect can occur is given by

$$N_s = \frac{N!}{(N - C_s)! C_s!} \quad (1.17)$$

where, N is the number of silicon atoms/cm³ and C_s is the concentration of schottky defects.

The entropy of the process is given by

$$s = k \ln N_s \quad (1.18)$$

The internal energy is given by the number of Schottky defects C_s , multiplied by the energy of Schottky defect formation E_s . The energy to form a Schottky defect is the energy to move an atom from a lattice position and out of the silicon ($\sim 2.3\text{eV}$).

The change in free energy neglecting volume changes is given by

$$F = E - TS = C_s E_s - kT [\ln N! - \ln C_s! - \ln(N - C_s)!] \quad (1.19)$$

The most probable equilibrium condition is the one where the free energy is a minimum with respect to changes in C_s , therefore

$$\left(\frac{\partial F}{\partial C_s} \right)_{T=\text{Const}} = 0 \quad (1.20)$$

Differentiating (1.19) and setting to zero

$$E_s = kT \frac{\partial}{\partial C_s} [\ln N! - \ln C_s! - \ln(N - C_s)!] \quad (1.21)$$

The factorial terms may be simplified by using Sterling's formula for the factorial of a large number. Therefore

$$\ln x! = x \ln x - x \quad (1.22)$$

and (1.21) reduces to

$$E_s = kT \ln \left(\frac{N - C_s}{C_s} \right) \quad (1.23)$$

or

$$C_s = \frac{N}{1 + e^{\frac{E_s}{kT}}} \cong N e^{-E_s/kT} \quad (1.24)$$

1.6.1.3.2. Frenkel defect concentration

Again assume only Frenkel defects are present in silicon. The number of ways a Frenkel defect can occur is given by

$$N_F = N_v N_i \quad (1.25)$$

where, N_v is the number of ways a vacancy can occur and N_i is the number of ways an interstitial can occur and the two are assumed to be statistically independent.

The entropy is given by

$$s = k \ln N_v N_i \quad (1.26)$$

The internal energy is given by

$$E = C_f E_f \quad (1.27)$$

where, C_f is the concentration of Frenkel defects and E_f is the energy of formation for a Frenkel defect ($\sim 1.1\text{eV}$).

The change in free energy is therefore

$$F = C_f E_f - kT \ln N_v N_i \quad (1.28)$$

As above

$$\left(\frac{\partial F}{\partial C_f} \right)_{T=\text{Const}} = 0 \quad (1.29)$$

in thermal equilibrium. Differentiating (1.28) and using Sterling's formula gives

$$E_f = kT \ln \left[\frac{(N - C_f)(N' - C_f)}{C_f^2} \right] \quad (1.30)$$

where, N' is the number of available interstitial sites per unit volume ($\sim 3 \times 10^{22}$ for silicon).
Or

$$C_f \cong \sqrt{NN'} e^{-E_f/2kT} = N e^{-E_f/2kT} \quad (1.31)$$

Under equilibrium conditions the concentration of vacancies and interstitials depends on all three-defect generation processes operating at the same time. The concentration of point defects at room temperature may exceed the expected value if the silicon was subject to higher temperatures and cooled quickly freezing in higher temperature point defect levels. Radiation and some integrated circuit processes can also generate point defects. It will be shown later in this book that ion implantation generates Frenkel defects, thermal oxidation can inject interstitials and thermal nitridation can inject vacancies. At elevated temperatures interstitial and vacancies can also recombine.

1.6.1.4. Point defect charges

The proceeding discussion of point defects has assumed that the point defects are electrically neutral. Vacancies can be electrically charged by capturing or releasing an electron



and interstitials can become electrically charged by the same mechanism



The concentration of charged vacancies relative to the concentration of neutral vacancies depends on the Fermi level and is given by [12]

$$C_V^+ = C_V^0 \exp[(E^+ + E_F)/kT] \quad (1.34)$$

$$C_V^- = C_V^0 \exp[(E_F - E^-)/kT] \quad (1.35)$$

$$C_V^{--} = C_V^0 \exp[(2E_F - E^- - E^{--})/kT] \quad (1.36)$$

where, C_V^0 is the neutral vacancy concentration and C_V^+ , C_V^- , C_V^{--} , are the positively, single negatively and double negatively charged vacancy concentrations respectively. E^+ , E^- , E^{--} , are the energy levels for the defects in the silicon energy gap, 0.35, -0.57 and $E_g + E^- - 0.11$ eV respectively [12].

The vacancy charge states and concentration are important considerations in diffusion theory as will be discussed in chapter 7.

1.6.2. Extended defects

Dislocations, twinning and stacking faults are three types of extended defects that may be generated during silicon processing.

1.6.2.1. Dislocations

During high-temperature processes mechanical stresses or thermal gradients may create strain in a silicon substrate, also high doping levels with dopants that have a size mismatch relative to silicon can introduce stress. For example, the thermal gradient strain induced in a substrate is given by

$$S = \alpha Y \Delta T \quad (1.37)$$

where, α is the coefficient of thermal expansion for silicon, Y is young's modulus, and ΔT is the temperature difference between the center and the edge of the substrate.

If the stress exceeds the yield strength of silicon a dislocation will form. Figure 1.18 illustrates the formation of an edge dislocation [11].

In figure 1.17a the crystal lattice is undisturbed, in figure 1.17b the lattice is under strain and in 1.17c through 1.17e the dislocation has formed and moves through the crystal along the

slip plane. Figure 1.18 illustrates the yield strength of silicon versus oxygen content [13]. The importance of oxygen content will be discussed further later in the chapter.

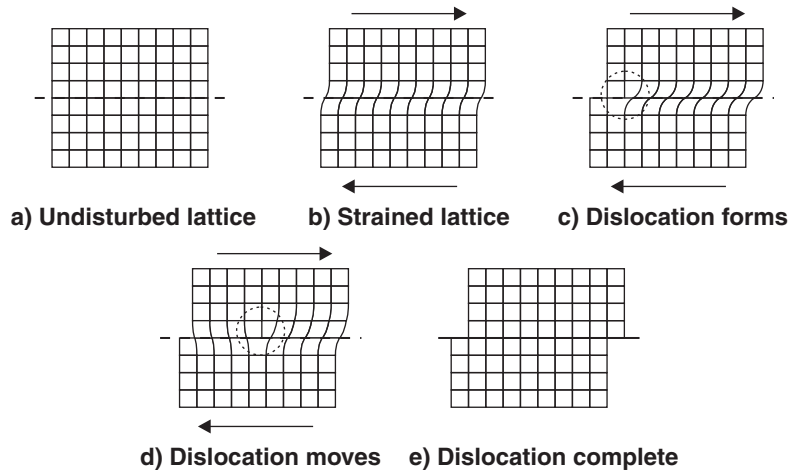


Figure 1.17: Edge dislocation formation [11].

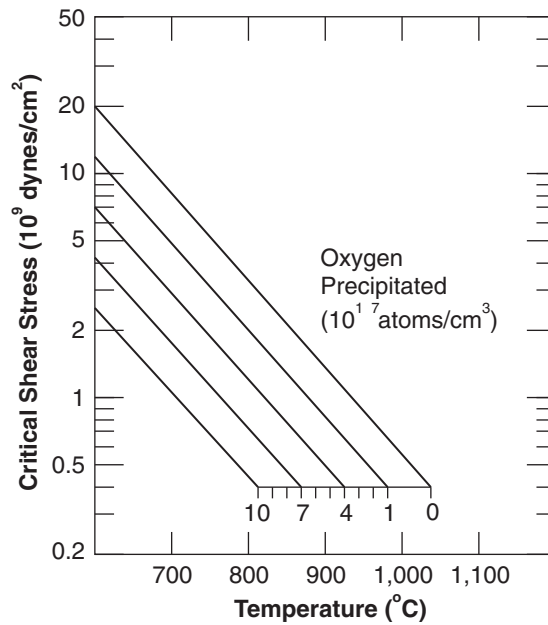


Figure 1.18: Yield strength of silicon versus oxygen precipitates [13].

1.6.2.2. Twinning

Twinning occurs when one portion of a crystal lattice takes up a different orientation with respect to another part of the lattice. Twinning is usually indicative of high levels of disloca-

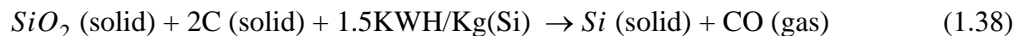
1.7.1. Substrate fabrication

The fabrication of commercial silicon substrates is a complex multi step process. Virtually all semiconductor manufacturers purchase silicon from commercial suppliers such as SEH, Sumitomo, Wacker or MEMC.

1.7.1.1. Polysilicon production

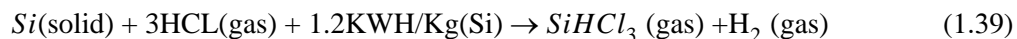
Commercial silicon production begins with the generation of electronic grade polysilicon. Polysilicon is made up of grains of single crystal silicon randomly oriented relative to each other (see chapter 9). There are four basic steps leading to electronic grade polysilicon [15].

1. An arc furnace is used with coal, coke or wood chips to reduce silica (SiO_2) with carbon in the following reaction

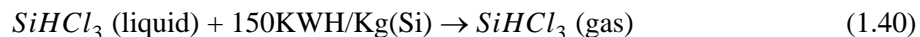


Silicon cooled down following this reaction is called metallurgical grade silicon and has a purity of approximately 98%.

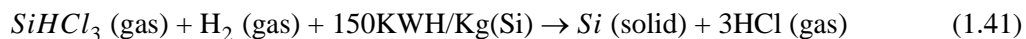
2. Powdered silicon is reacted with hydrogen chloride (HCl) in a fluid bed to form trichlorosilane (SiHCl_3) by the following reaction



3. The trichlorosilane is purified by distillation to yield electronic grade purity. The reaction is



4. Finally in a reductive and pyrolytic reaction with high purity hydrogen the trichlorosilane is turned into high purity silicon. The silicon is deposited in the form of a large polycrystal. The reaction is given by



1.7.1.2. Crystal growth

The polycrystalline silicon produced in the process described above must be converted into single crystal form for use in IC fabrication. There are two techniques utilized to grow single crystal silicon, Czochralski (CZ) or float zone (FZ). Table 1.3 compares the silicon crystal purity produced by the two methods.

From table 1.3 one might expect that float zone would be the crystal growth method of choice due to higher purity. In fact Czochralski dominates the production of commercial silicon. As will be seen in section 1.7.4 the higher oxygen content present in CZ wafers can be turned to an advantage creating internal gettering sites. Due to the dominance of CZ growth techniques FZ will not be discussed further.

Table 1.3: Impurity content in typical silicon crystals [16].

Impurity	Float zone (atoms/cm ³)	Czochralski (atoms/cm ³)
Calcium	2.71×10^{15}	2×10^{16}
Carbon	2.2×10^{16}	1.5×10^{17}
Chlorine	10^{15}	10^{15}
Cobalt	$< 10^{15}$	$< 10^{15}$
Copper	8.5×10^{15}	1.9×10^{16}
Fluorine	1×10^{16}	2×10^{16}
Iron	$< 10^{15}$	10^{16}
Manganese	$< 10^{15}$	$< 10^{15}$
Nickel	$< 10^{15}$	$< 10^{15}$
Oxygen	3×10^{16}	4×10^{17}
Potassium	$< 10^{15}$	$< 10^{15}$
Sodium	1.5×10^{15}	10^{15}

Figure 1.21 illustrates a CZ crystal puller.

The Czochralski technique is named after the inventor. The technique uses a small seed crystal, which is dipped into a molten silicon bath and slowly withdrawn. The molten silicon bath is rotated in one direction and the growing silicon “boule” is rotated in the opposite direction. For very large crystal growth the silicon melt is continuously replenished. The silicon melt includes impurities deliberately introduced to dope the silicon. The growing boule is formed in an inert argon atmosphere to prevent contamination.

1.7.1.3. Wafer formation

Once the single crystal silicon boule is formed a number of operations are performed to create the silicon “wafers” utilized in IC fabrication. Figure 1.22 summarizes the silicon wafer manufacturing process.

The wafer manufacturing steps illustrated in figure 1.22 are as follows:

1. Pull Crystal Ingot - A small seed of single crystal silicon is dipped into a crucible of molten silicon. The crucible and seed are rotated in opposite directions and the seed is slowly withdrawn from the crucible - figure 1.22a. As described above.

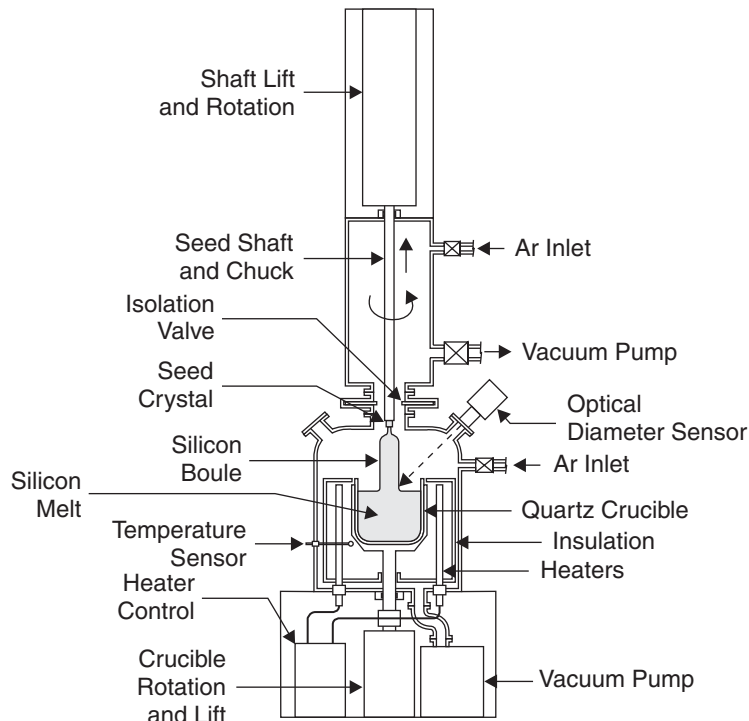


Figure 1.21: Czochralski crystal puller.

2. Ingot Grind - The silicon crystal ingot is ground to create a consistent diameter for the whole ingot - figure 1.22b.
3. Saw Off Ingot Ends - The two ends of the silicon ingot will not be usable and are sawn off using a diamond saw - figure 1.22c.
4. Saw Up Ingot Into Wafers - The Ingot is sawn up into wafers each approximately 1/2mm to 3/4mm in thickness - figure 1.22d.
5. Edge Grind Wafers - The edges of the wafers are ground to round off the sharp edges. Edge grinding minimizes chipping of the wafer edges during subsequent processing - figure 1.22e.
6. Lap Wafers - A process called lapping is used to flatten out the wafers and ensures the two wafer faces are parallel - figure 1.22f.
7. Damage Removal Etch - A special wet etch is used to etch off the surface damage left from lapping - figure 1.22g.
8. Polish - The polish step removes the final residual damage layer on the wafers and creates a mirror polish surface - figure 1.22h.
9. Final Clean - The final clean step removes any contaminants left on the wafer surface from the previous steps - figure 1.22i.

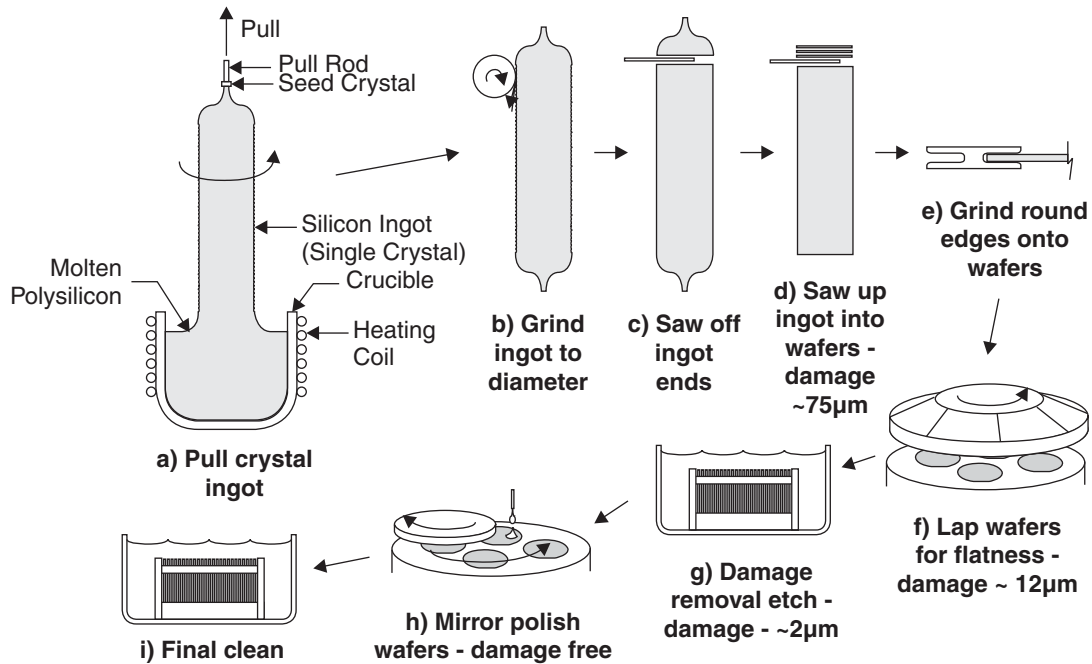


Figure 1.22: Silicon wafer manufacturing process [17].

1.7.2. Substrate dimensions and orientation

Silicon wafers are discs of a standard diameter and thickness defined by standards published by SEMI [18]. The diameter of wafers in production use has evolved over the years from 50mm (~1/2") wafers to the current volume leader 200mm (8") wafers. Figure 1.23 presents the worldwide silicon wafer use by size versus time.

Figure 1.23 illustrates two important trends:

1. First, the diameter of silicon wafers is increasing. Larger diameter wafers allow more individual circuits to be fabricated per wafer simultaneously. There are a number of factors involved in IC production costs, but generally speaking larger wafer sizes result in lower production costs per individual IC, this trend is particularly strong for state-of-the-art ICs. Of course each new wafer size requires extensive and expensive retooling.
2. The second trend is the continuous increase in the total amount of silicon consumed. As was discussed in the introduction the semiconductor industry continues to grow at a rapid rate.

Silicon wafers are generally available as (100) or (111) orientation. The type of wafer and crystal orientation can be determined from the position of the primary and secondary flat on the wafer. Flats as the name implies are flat areas in the wafer circumference used to orient the wafer during processing. Figure 1.24 illustrates the wafer flat convention.

The wafer flats defined in figure 1.24 are valid for wafer sizes smaller than 150mm, at 150mm the (100) p-type wafer secondary flat was moved to 135° . At 200mm only a primary flat is used for orientation since virtually all 200mm wafers are (100) p-type (boron doped). Furthermore, many 200mm wafers are produced with a small notch in place of a flat for orientation.

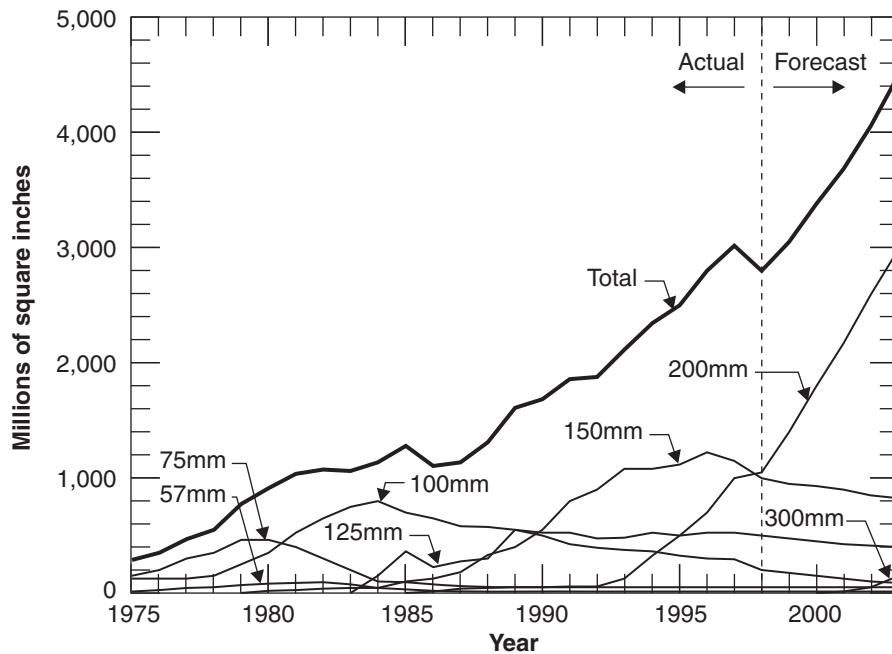


Figure 1.23: Silicon wafer diameter trends.
Figure courtesy of Rose Associates.

Table 1.4 presents the dimensions of SEMI standard wafer sizes [18]. Note the table 1.4 does not list a second flat orientation for p(111) wafers because a second flat is not used.

1.7.3. Gettering

During the process of fabricating integrated circuits it is virtually impossible to prevent metallic contamination of the silicon. Metallic impurities including iron, chromium, copper and nickel can lead to degraded electrical performance such as lower carrier mobility, poor gate oxide quality and junction leakage. In order to tie up metallic impurities and prevent them from contaminating the wafer surface area where devices are fabricated, some form of gettering technique is frequently used. There are two main types of gettering, internal and external.

1.7.3.1. External gettering

External gettering is accomplished by creating a damage layer at the back of the wafer. The damage layer attracts and traps impurities. Backside gettering techniques include damage layer formation by argon ion implantation, sand blasting the back surface or deposition of backside

polysilicon. The long distance from the front side devices to the backside damage layer and the tendency of backside damage to anneal out limits the effectiveness of external gettering.

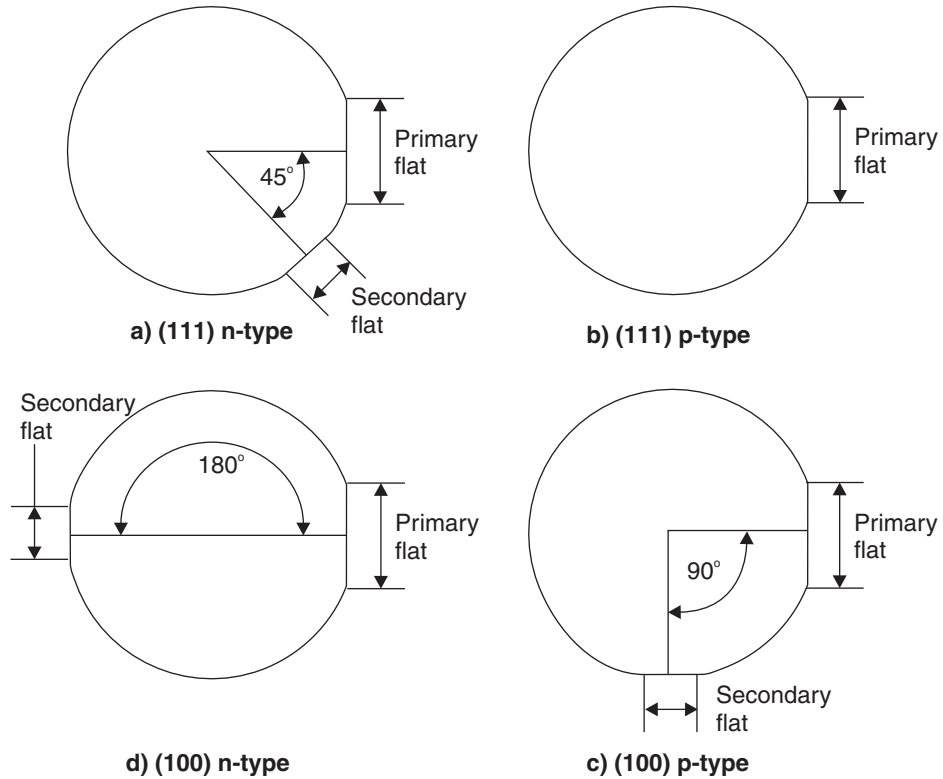


Figure 1.24: Wafer flats [19].

Table 1.4: Standard wafer sizes [18].

Wafer size	Diameter (mm)	Thickness (μm)	Primary flat (mm)	Second flat (mm)
2"	51	279	15.88	8.00
3"	76	381	22.22	11.18
100mm	100	525	32.50	18.00
125mm	125	625	42.50	27.50
150mm	150	675	57.50	37.50
200mm	200	725	95.50	none
300mm	300	780	notch	none
450mm	450	880 est.	notch	none

1.7.3.2. Internal gettering

The high oxygen content in CZ grown silicon wafers can be used to form internal gettering sites. There are three requirements to obtain internal oxygen gettering:

1. High oxygen content in the wafer - 5×10^{17} to 1×10^{18} oxygen atoms/cm³.
2. Create an oxygen denuded zone at the wafer surface. The denuded zone is a low oxygen concentration region deeper than the deepest active device region (typically the wells for CMOS).
3. Grow oxygen precipitates in the bulk of the wafer.

Figure 1.25 schematically illustrates a wafer with internal oxygen gettering.

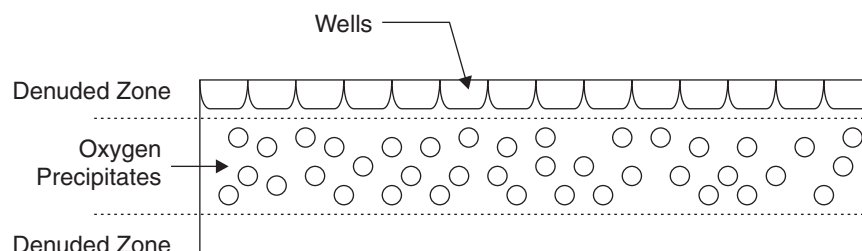


Figure 1.25: Schematic diagram of oxygen internal gettering [17].

In order to create the gettering structure illustrated in figure 1.25 a two step process is used. First a high temperature step is used to diffuse oxygen out from the wafer surfaces. Above 950°C oxygen diffusion with denuded zone formation is favored over oxygen nucleation and precipitate growth. Once a denuded zone is formed oxygen is nucleated with a thermal step below 950°C where nucleation is favored over diffusion. A third step to grow the oxygen nuclei into large precipitates may also be used.

Figure 1.26 illustrates the rate of nucleation and the denuded zone thickness versus temperature. The denuded zone is typically formed to a depth deeper than the deepest active device area and the oxygen content must be $< 2 \times 10^{17}$ - the critical oxygen level for precipitate formation. Oxygen precipitates in the active device area degrade performance and yield.

Figure 1.27 schematically illustrates the oxygen concentration profile through a denuded zone.

Well depth for CMOS with 250nm feature sizes is approximately 1.5µms. The denuded zone must therefore be $> 1.5\mu\text{ms}$. In order to insure the highest quality devices the denuded zone is designed to be several µms deeper than the deepest active area. From figure 1.26, a 2-hour steam cycle will accomplish the required denuded zone depth at temperatures as low as 1,000°C.

A denuding zone formation and oxygen precipitation cycle for state-of-the-art CMOS is as follows:

- Purchase high oxygen content wafers - 5×10^{17} to 7.5×10^{17} oxygen atoms/cm³.
- Denude the wafer surface of oxygen - 3 to 4 hours at 1,100°C in a 1% HCl in O₂ atmosphere. The HCl suppresses stacking fault formation and promotes cleanliness (see chapter 4).
- Nucleate oxygen - 1 hour at 800°C.

- Grow oxygen nuclei into precipitates at $\sim 1,000^{\circ}\text{C}$. The growth process may be skipped if subsequent thermal processes will grow the nuclei. Ideally precipitates of approximately 5nm in diameter should be grown. The oxygen precipitates create a volume mismatch with silicon forming stacking faults and dislocations that trap impurities.

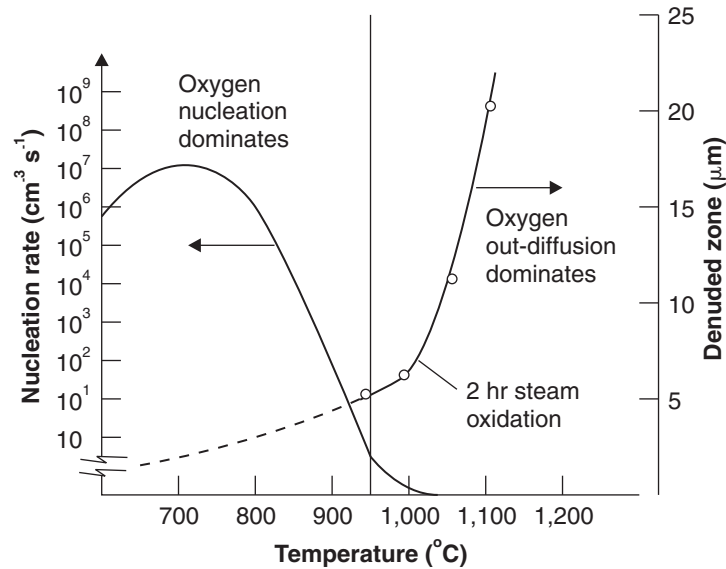


Figure 1.26: Oxygen nucleation rate and denuded zone depth versus temperature [19].

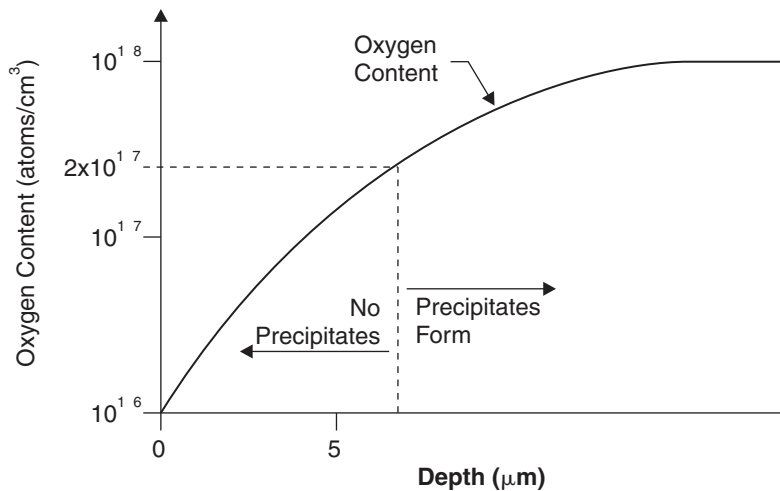


Figure 1.27: Oxygen profile through a denuded zone [17].

Highly doped boron regions may provide additional gettering of iron. Current state-of-the-art practice calls for boron doped substrates. When an epitaxial layer is to be used (see chapter 9), a highly boron doped substrate is used, if a bulk wafer is used a lighter boron doping layer is

required. Some fabrication processes utilize lightly doped boron substrates with a heavily doped boron buried layer to enhance device performance and getter impurities.

1.7.4. Crystal originated particles

The term crystal originated particle or COP is a bit of a misnomer. A COP is a defect in the silicon surface that “appears” to be a particle to an automated surface particle scanners. COPs are small voids in silicon formed by vacancy clusters during crystal growth. COPs can degrade the integrity of critical gate oxide layers grown on the silicon surface (gate oxide integrity or GOI). During crystal growth vacancies or interstitials form with the dominant defect determined by the crystal growth conditions. The dominant defect depends on [20]

$$\xi = V/G_0 \tag{1.42}$$

where: V is the crystal growth rate and G_0 is the near interface axial temperature gradient.

Vacancy generation dominates when

$$\xi > \xi_t \tag{1.43}$$

and interstitial generation dominates when

$$\xi < \xi_t \tag{1.44}$$

where for silicon $\xi_t \sim 0.12\mu\text{m}^2/\text{min K}$.

When $\xi \gg \xi_t$ or $\xi \ll \xi_t$, point defect concentrations of $\sim 10^{14}/\text{cm}^3$ will be generated.

COPs may be minimized during crystal growth by slow cooling the silicon in the temperature range around 1,100°C [21]. COPs may also be reduced through the use of high temperature anneals (see figure 1.28).

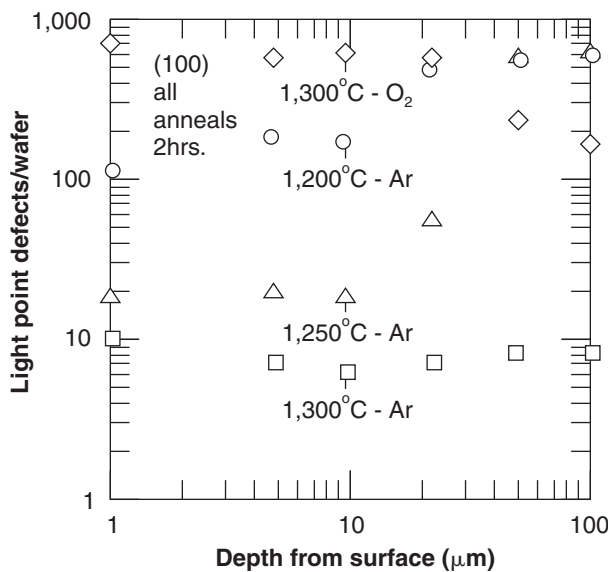


Figure 1.28: Number of LPDs versus depth and anneal [22].

Figure 1.28 illustrates light point defects which may be COPs or actual particles for 150mm - (100) silicon after a variety of 2 hour anneals. The defect level was characterized for surface defects and also versus depth by polishing into the crystal and measuring defects at various depths. For current state-of-the-art 0.18 μ m wafer fabrication the goal for COPs is < 38/200mm wafer (21 COPs/150mm wafer) [22]. As linewidths continue to shrink slow cooled silicon and annealing techniques to reduce COP levels will become increasingly critical.

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Problems

1. Calculate the doping level required to make silicon an extrinsic semiconductor at room temperature.
2. For silicon with a doping concentration of $5 \times 10^{16}/\text{cm}^3$ calculate, a) the mobility of holes if the dopant is boron, b) the mobility of electrons if the dopant is phosphorus, c) the fermi level relative to the valence band if the dopant is boron.
3. Calculate the point defect concentration due to Frenkel and Schottky defects at 500°C for silicon.
4. Describe internal gettering and the critical factors to consider when setting up an internal gettering process.
5. Describe a COP, what problems a COP causes and two strategies for minimizing COP levels.