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Technology backgrounder: High-k gate oxides

1.0. Introduction

Since it's inception, the semiconductor industry has been driven by constantly increasing transistor counts and performance per integrated circuit (IC). The single biggest driver has been continually shrinking linewidths that have allowed more and more transistors to fit into the same area and simultaneously improve performance. Historically linewidths have shrunk every three years, and recently linewidths have been shrinking every two years - see figure 1.

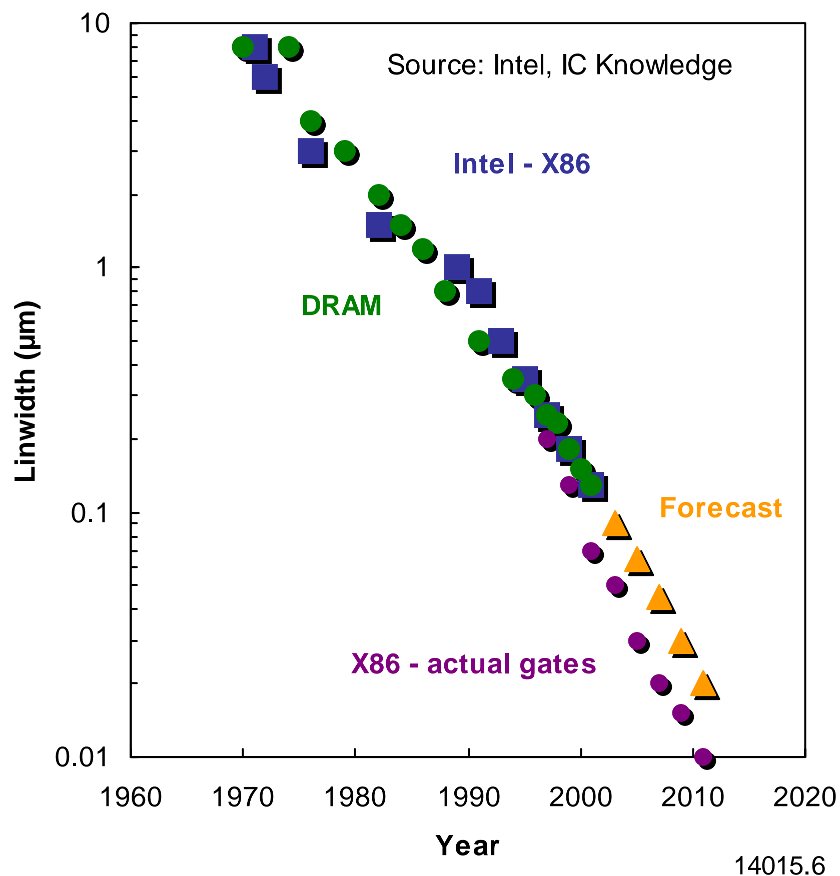

Figure 1. Lithography rules trends.

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In figure 1, the blue squares represent the linewidths for Intel microprocessors and the green circles represent DRAMs, the orange triangles represent IC Knowledge's forecasts for the next several years and the purple circles are the actual physical gate lengths of transistors on the Intel microprocessors. Note how the physical gate lengths have diverged to roughly ½ the size of the "lithography rule linewidths"!

In 1972 Bob Dennard of IBM discovered MOSFET scaling [1]. The basic concept of scaling is that if you maintain a constant electric field while shrinking a MOSFET, all other performance parameters improve while producing a smaller device. For example, if you shrink the gate length of the device by 1/k and reduce the operating voltage by 1/k, a constant electric field results and the circuit delay is also reduce by 1/k. So for a 250nm gate length MOSFET scaled by k=1.4, the new gate length is 180nm, the operating voltage drops from 1.8 to 1.3 volts and the circuit delay becomes 0.7x of what is was at 250nm. Since operating frequency (the Megahertz that are so popular) increases as circuit delay decreases, the operating frequency becomes 1.43x whatever it was at 250nm. If we assume a 800MHz frequency at 250nm, then in theory 180nm processing should yield 1.1GHz. The effect of shrinking linewidths on transistor size is actually proportional to the linewidth squared since transistors have length and width and both are shrinking. A 180nm transistor should therefore be roughly 50% of the size of a 250nm transistor allowing twice as many transistors to be packed into the same size IC.

In order to produce a smaller transistor it is not sufficient to just shrink the transistors physical length and width, other dimensions must be shrunk as well. Shrinking gate lengths L_G, require thinner sidewall spacers X_S, shallower junctions X_{JE} and X_{JC}, and most importantly for the purpose of this article, thinner gate oxides X_G - see figure 2.

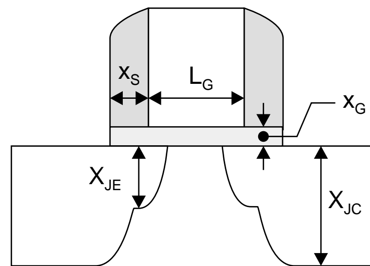

Figure 2. MOSFET dimensions for physical scaling [2].

In the past, gate oxides have been shrinking in thickness right along with gate length shrinks. Intel gate oxides have shrunk over the last 20 years by [3]:

$$X_G = L_G/45 \quad (1)$$

With actual L_G reaching 70nm, X_G is now less than 2nm. With 2nm only representing some 6 to 7 atomic layers of silicon dioxide (SiO_2), silicon dioxide is less and less like a good insulator and electrical leakage is increasing unacceptably.

2.0. Effective oxide thickness

The gate oxide thickness required for good MOSFET control actually depends on the capacitance of the film. Capacitance is given by:

$$C = \frac{k\varepsilon A}{t} \quad (2)$$

where, k is the dielectric constant, A is the area and t is the thickness.

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Silicon dioxide (SiO_2) has a k value of 3.9, if an alternate material could be found with a higher k value, then the same capacitance per unit area A could be achieved with a physically thicker film and potentially lower leakage.

Comparison of various films and the thickness that would result is done using the concept of equivalent oxide thickness (EOT). EOT is given by:

$$EOT = (k_{SiO2}/k_x)t_x \quad (3)$$

where, k_x is the k value for the film of interest, t_x is the physical thickness of the film of interest and k_{SiO2} is the k value of silicon dioxide. From equation 3, a film with a k value of 7 could be almost twice as thick as a silicon dioxide film with a k of 3.9 and still have the same control over the MOSFET.

3.0. High-k films

There are a wide variety of films with higher k values than SiO_2, ranging from Si_3N_4 with a k value of 7, up to Pb-La-Ti (PLT) with a k value of 1,400. Unfortunately many of these films are not thermodynamically stable on silicon, or are lacking in other properties such as a high breakdown voltage, low defect density, good adhesion, thermal stability, low deposition temperature, ability to be patterned easily and low charge states on silicon.

Currently interest seems to be centered on films such as HfO_2 and ZrO_2 with k values of 30-40 and 25 respectively, enabling a 6.4x to 10.3x increase in film thickness for equivalent performance. Intel recently reported over five orders of magnitude reduction of leakage for high-k oxides based on HfO_2 and ZrO_2 versus SiO_2 for equivalent oxide thicknesses [4]. Transistors based on these films showed excellent overall performance presenting possible solutions to the need for thinner EOT with low leakage.

It should be pointed out here that high-k use as a gate oxide is distinct from high-k use in DRAM capacitors. In a DRAM capacitor, the objective is to maximize capacitance per unit area. The capacitor is frequently fabricated after the transistors and sees less thermal processing. DRAM capacitor oxides can be sandwiched between various electrode materials that allow high-k materials to be used that can’t be used as a gate oxide where contact with silicon is a requirement.

4.0. Conclusion

High-k oxides offer a solution to leakage problems that occur as gate oxide thickness’ are scaled down. By using an electrically equivalent thickness of high-k oxides, leakage may be reduced by over 5 orders of magnitude allowing continued scaling of MOSFETs. Currently, we at IC Knowledge expect that the 90nm generation due to 2003 will continue to have SiO_2 gates, but that the 65nm generation due in 2005 will require high-k gate oxides.

References

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[2] Scotten W. Jones, *“Fundamental Principles of Integrated Circuit Fabrication,”* Unpublished.

[3] Scott Thompson, Paul Packan and Mark Bohr, *“MOS Scaling: Transistor Challenges for the 21st Century,”* Intel Technol. J., Q3 (1998).

[4] Doug Barlage, Reza Arghavani, Gilbert Dewey, Mark Doczy, Brian Doyle, Jack Kavalieros, Anand Murthy, Brian Roberds, Pat Stockley and Robert Chau, *“High Frequency Response of Transistor with High-K Gate Dielectrics,”* http://www.intel.com/research/silicon/HighKfoils.pdf

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